

3 GHz digital rf control at the superconducting Darmstadt electron linear accelerator: First results from the baseband approach and extensions for other frequencies

A. Araz,^{*} U. Bonnes, R. Eichhorn, F. Hug, M. Konrad, M. Platz, and A. Richter[†]

TU Darmstadt, D-64289 Darmstadt, Germany

R. Stassen

Forschungszentrum Jülich, D-52425 Jülich, Germany

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The low level rf system for the superconducting Darmstadt electron linear accelerator (S-DALINAC) developed 20 years ago and operating since converts the 3 GHz signals from the cavities down to the baseband and not to an intermediate frequency. While designing the new, digital rf control system this concept was kept: the rf module does the I/Q and amplitude modulation/demodulation while the low frequency board, housing an field programmable gate array analyzes and processes the signals. Recently, the flexibility of this concept was realized: By replacing the modulator/demodulators on the rf module, cavities operating at frequencies other than the one of the S-DALINAC can be controlled with only minor modifications: A 6 GHz version, needed for a harmonic bunching system at the S-DALINAC and a 324 MHz solution to be used on a room temperature cavity at GSI, are currently under design. This paper reviews the concept of the digital low level rf control loops in detail and reports on the results gained during first operation with a superconducting cavity.

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I. INTRODUCTION

The superconducting Darmstadt electron linear accelerator (S-DALINAC) [1] is a recirculating linac with beam currents of up to $60 \mu\text{A}$ and a maximum energy of 130 MeV. It is primarily used for experiments in nuclear physics since it has been first put into operation in 1987. The layout of the S-DALINAC is shown in Fig. 1. In order to reach this energy ten 20-cell, one 5-cell, and one 2-cell superconducting (sc) niobium cavities, operating at 2 K and a frequency of 3 GHz, are used. The design quality factor Q is 3×10^9 at an accelerating gradient of 5 MV/m. Even when the sc cavities are strongly coupled with a loaded quality factor of 3×10^7 , which leads to a resonance width of some 100 Hz, they are very sensitive against microphonic perturbations [2]. In order to achieve the recommended energy spread of $\pm 1 \times 10^{-4}$ at the experimental areas, the amplitude and phase of the cavities have to be controlled strictly to compensate the impact of microphonic perturbations. This compensation has to be done by the low level rf control system reaching the stability specifications given in Table I.

II. CONTROL LOOP PRINCIPLE

The rf control system at the S-DALINAC uses a self-excited loop (SEL) [3,4] to control the amplitude and phase of the sc cavities. A simplified scheme of the rf control loop

is shown in Fig. 2. The SEL starts to oscillate from noise even when the resonator frequency does not match the generator frequency, if the loop gain is greater than 1 and if the loop phase is a multiple of 2π . To ensure this, the loop phase is adjusted by the phase shifter within the main signal path.

The cavity signals are measured and analyzed with two different detectors. The amplitude is detected directly with a linear detector. After subtraction of the set point the error signal is generated. Because of the fact that the I/Q domain is used to process the phase inside the existing control loop a complex phasor modulator (CPM) [5], which has the inverse transfer function of the cavity and thus decouples (ideally) the amplitude and phase characteristics of the loop, is used to control the phase. The phase modulation is done by adding a small orthogonal vector to the loop vector. The amplitude modulation is accomplished by a simple proportional controller, which amplifies the amplitude error signal. This new amplitude control signal

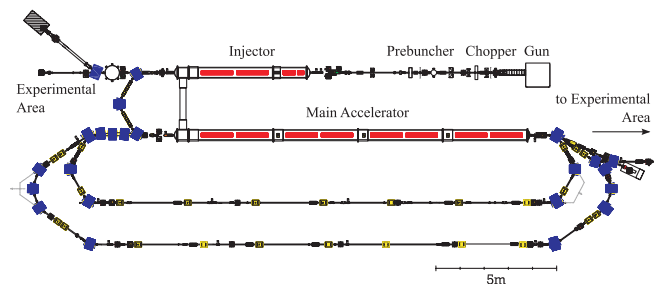


FIG. 1. (Color) Floor plan of the S-DALINAC.

^{*}araz@ikp.tu-darmstadt.de

[†]Also at ECT*, Villa Tambusi, I-38100 Villazzano, Trento, Italy.

TABLE I. Stability specifications.

| | | |
|------------------------------|------------------|------------------------|
| Relative amplitude stability | $\Delta E/E$ | $\pm 8 \times 10^{-5}$ |
| Phase stability | $\Delta \varphi$ | $\pm 0.7^\circ$ |

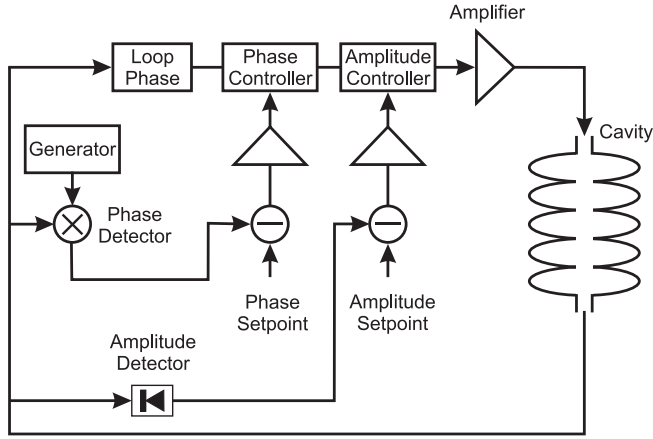


FIG. 2. Self-excited loop diagram.

is modulated by a simple multiplication onto the I/Q signals. Finally, the new control signals are amplified and sent back to the cavity.

III. PRESENT RF CONTROL SYSTEM

The low level rf control system for the S-DALINAC consists of two main parts: In the rf board the 3 GHz signals are converted down to the baseband and not to an intermediate frequency like elsewhere [6]. The analysis and the control of the baseband signals is done by a low frequency module, which was built with analogue components. These control loops performed quite well, leading to a high quality beam, which for example was essential for the success of the free electron laser operation in the 1990's [7]. Nevertheless, the maintenance effort of the existing system has become more difficult in time because of the aging of all components. In addition, new experiments at the S-DALINAC put more demanding constraints on the energy spread of the beam. As a consequence, the design of a new control system was carried out making use of modern components offering better performance and stability.

IV. NEW RF CONTROL SYSTEM

A. Layout

The concept of the newly developed rf control system follows the existing design described above and shown in Fig. 3. The high frequency cavity signal is converted down to the baseband by an rf board, again. The low frequency signals, amplitude and the demodulated I/Q phasors are transmitted as analogue signals to the new field programmable gate array (FPGA) board, where they are digitized

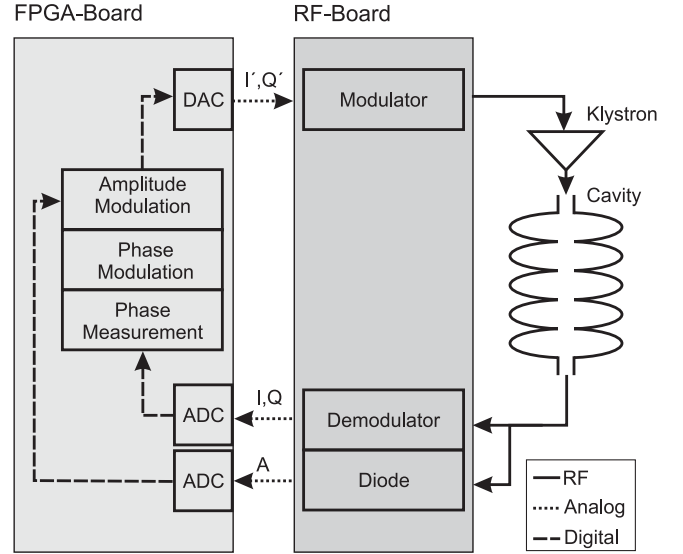


FIG. 3. Layout of the new rf control system.

and processed. After the algorithm is applied, the signals are transformed to analogue again and transferred to the rf board where they are modulated onto the 3 GHz LO frequency to drive the cavity.

B. FPGA board

Following the mainstream in rf control-system design for the new low frequency module, a digital solution based on an FPGA (Xilinx Spartan 3) has been developed. The great flexibility of a digital solution is one of the most important features. The same hardware can be used to realize different or more complex control loops. These loops are developed with VERILOG and programmed into the FPGA. The changes are analyzed and the control accuracy can be compared directly.

The developed module is shown in Fig. 4. The FPGA has a main clock of 80 MHz, which allows one to digitize and to process the analogue low frequency signals from the rf board with a sampling rate of 1 M samples per second. The analog-to-digital converters (ADCs) have a measured resolution of 16 bits. The implemented USB 2.0 interface is used for an extensive diagnostics of the control loop. This interface allows one to read out up to eight parameters inside the control loop in real time and with high resolution without data reductions. During the first operation, a software oscilloscope was used to visualize the control loop parameters and to record the data. This allows an off-line data analysis, which is important for the optimization of the control parameters. Those control parameters, like amplification gain inside the control loop, were set via a CAN-bus interface.

C. RF board

The printed circuit of the new rf module is shown in Fig. 5. The board is built out of RO4350, a high frequency

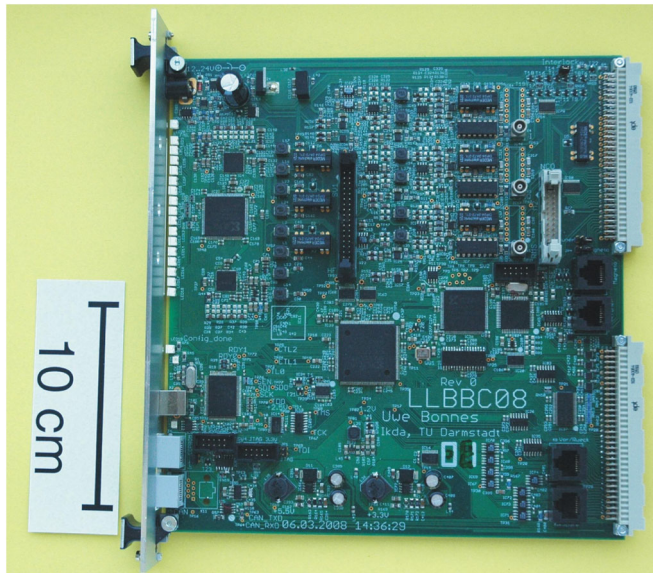


FIG. 4. (Color) Picture of the FPGA board.

capable Rogers material. It consists of highly integrated, commercially available Wi-Fi components with low noise and excellent stability against temperature variation.

A scheme of the new rf module is presented in Fig. 6. The rf module houses an I/Q demodulator (AD8347) as well as an amplitude detector (ADL5500), which meet the design constraints.

Once the FPGA module has generated the new I/Q signals, they are modulated (ADL5374) onto the rf reference. A variable attenuator (SKY 12146-321) located downstream the I/Q modulator allows one to set the loop gain, which is necessary to compensate changes induced by coupling variations of the cavities. The up-conversion and down-conversion of the rf signal is done by three complex circuits, which require only a few connections and some additional components including the directional couplers (1P610, 1P620).

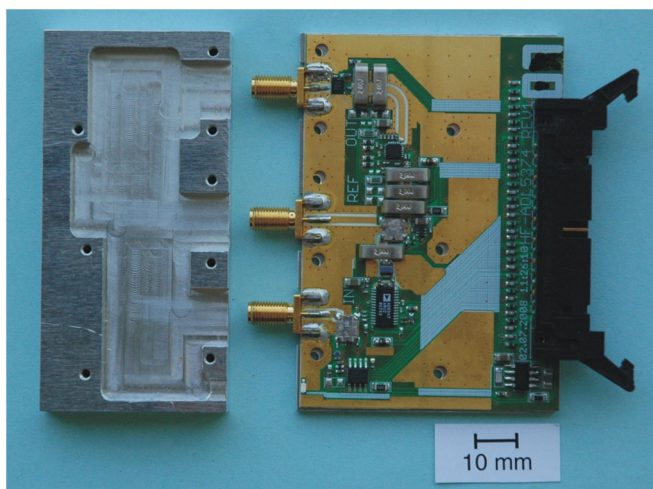


FIG. 5. (Color) Picture of the new rf board.

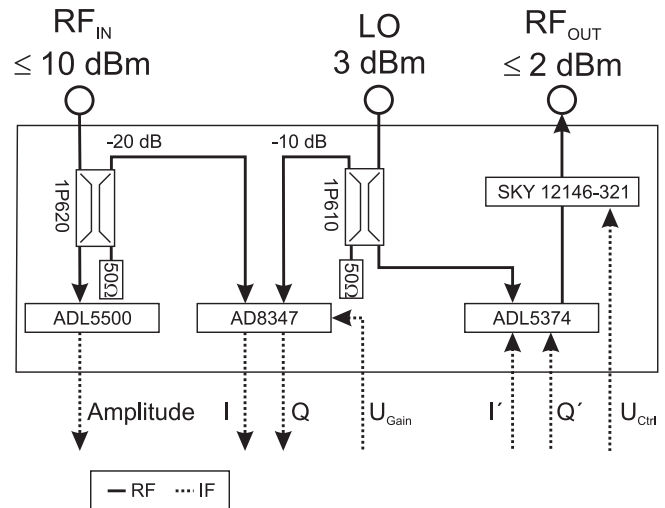


FIG. 6. Functional diagram of the new rf board. The integrated circuits are described in the text.

By changing the couplers and the modulator, a 1.3 GHz version was built and tested. Currently, a 6 GHz version, needed for a harmonic bunching system, is under design [8]. Furthermore, a 324 MHz solution to be used on a room temperature cavity at GSI will be developed. While the 1.3, 3, and 6 GHz versions will operate in a cw mode, the 324 MHz board has to be capable of pulsed operation.

D. Control algorithm

As a first design step the FPGA-based prototype was built [9]. The control algorithm, programmed into this prototype, is the mathematical representation of the existing analogue control loop (Fig. 2).

The performance and the control accuracy of the prototype reached the performance of the analogue system easily. In a second step, a scalable system was designed, which is presented above. Meanwhile, the control algorithm has been improved in order to reach a better performance.

A simplified scheme of this improved control algorithm is shown in Fig. 7. It starts (on the top) with the readout of the ADC channels for the amplitude (A) and the Cartesian phase coordinates (I and Q). The amplitude control loop uses a separate detector to increase the accuracy. After the subtraction of the set point a proportional and an integral controller is used to process the error signal and to generate the new control signal. The phase control loop is done in a more complex way than in the existing control system. In order to realize the phase controller similar to the amplitude controller (proportional and integral controller), the new phase modulation changes the domain from I/Q into phase and amplitude. Therefore an iterative algorithm, which is called coordinate rotation digital computer (CORDIC) [10], converts the Cartesian (I/Q) to polar (phase and amplitude) coordinates. The fast phase errors,

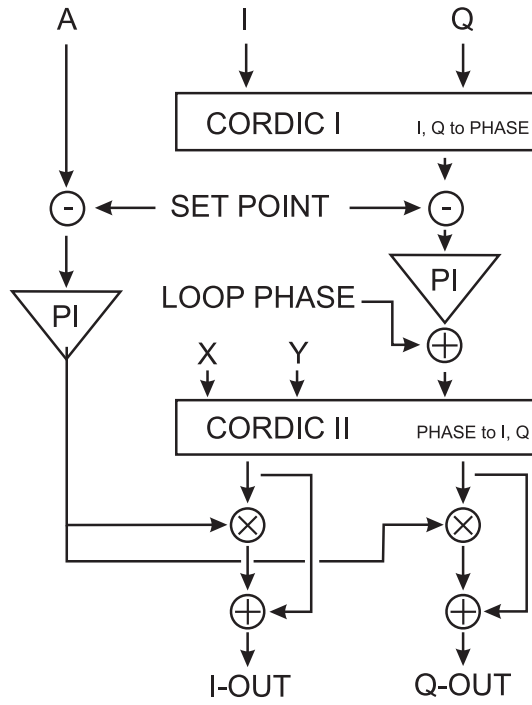


FIG. 7. Diagram of the new algorithm.

resulting from perturbations of the cavity, are corrected by the phase controller. In addition, the slow phase changes, produced by a frequency change of the cavity, have to be corrected via a tuning system. After the phase processing the domain is changed back with a second CORDIC to I/Q domain again. The last step is the amplitude modulation. The amplitude control signal has a range from -1 up to 1 . To avoid a mirroring of the I/Q signal created through a negative amplitude control signal, the previous I/Q signals are added on the amplitude modulated I/Q signals, which takes care that the output signal will be zero if the amplitude is to high.

The new control algorithm can be used as a SEL, if the input vectors for the first and second CORDIC are the same vectors ($X = I$, $Y = Q$). Furthermore it is possible to use the same algorithm as generator driven resonator, if a constant vector is used as input for the second CORDIC ($X = 1$, $Y = 0$), which is important for the operation of normal conducting copper resonators with low Q used in the low energy part of the injector of the S-DALINAC. Even the system looks rather smart, the programming took several months and many iterations, until the right parameter settings were found and optimized.

E. Performance

During the testing, the performance of the new control loop was quantified. The control parameters were set via a CAN-Bus interface. To have no data reduction within the data acquisition, the FPGA board was read out via an USB interface, which allowed observing several parameters in real time with a high resolution.

To prove the performance of the new rf control system under realistic conditions a standard 20-cell cavity located inside the injector linac was driven by the new system. The cavity had a loaded quality factor of some 3×10^7 and the amplitude was set to 3 MV/m . To have a typical operating situation a beam current of $20 \mu\text{A}$ was accelerated. To keep the control loop as simple as possible and to reduce the control parameters, during the first measurements with the new system, only the proportional controller of the phase controller was activated. Figure 8 shows the observed control accuracy. The amplitude controller, which consists of a proportional and an integral controller, was able to lock his set point and no residual offsets were observed. The measured relative amplitude stability was about 2.3×10^{-4} (rms). The phase controller was able to lock the phase with an accuracy of about 0.3° (rms), but a residual phase offset of about 1.3° was observed (indications for the necessity of an integral controller).

Once the parameter settings and some experiences with the new system were gained, the integral controller within the phase loop was activated. The resulting measured control accuracy is shown in Fig. 9. In the course of the testing, the amplitude and phase were locked to their set points and no residual offsets were observed. The measured phase stability of about 0.3° (rms) fulfilled the

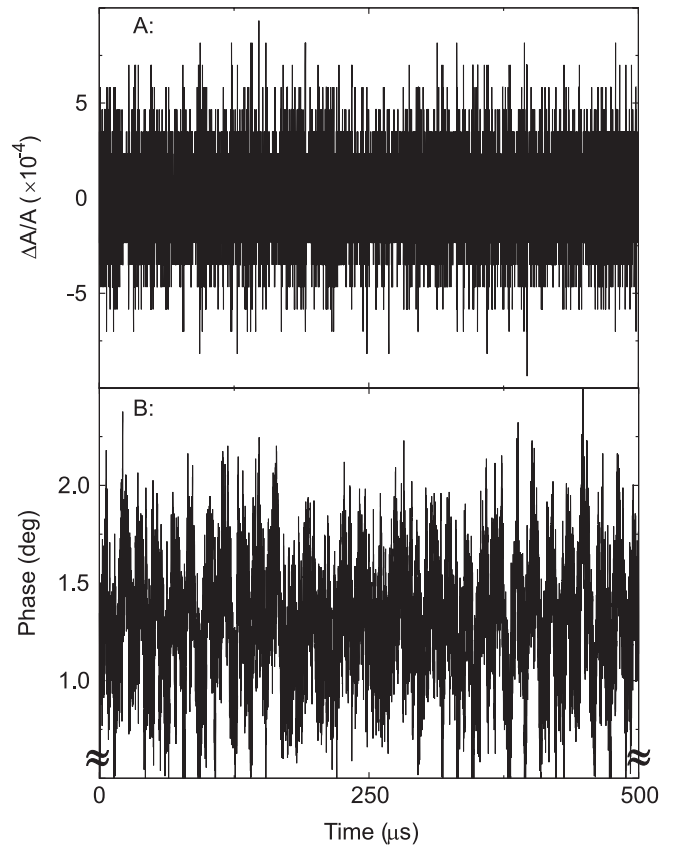


FIG. 8. Amplitude (A) and phase (B) error of the digital control system without an integral controller in the phase loop.

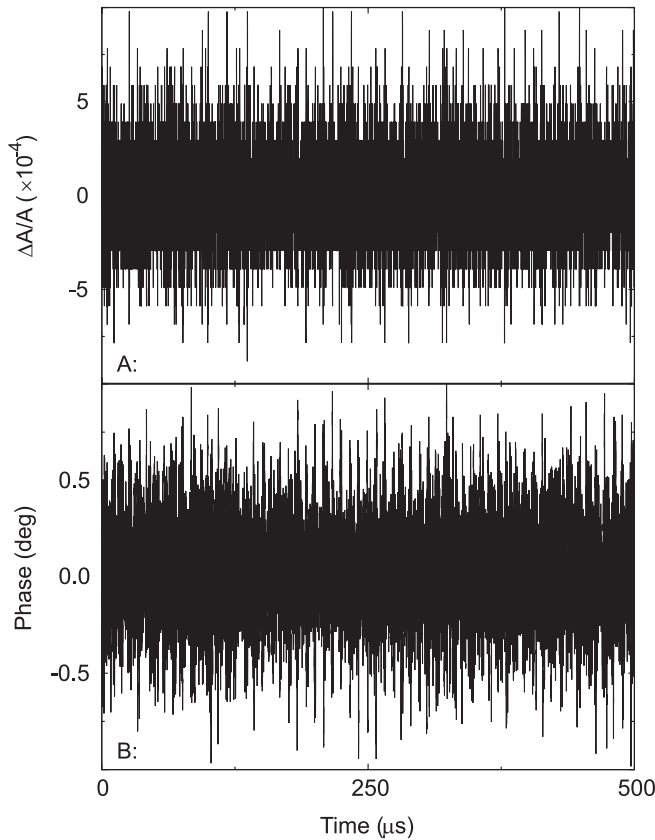


FIG. 9. Amplitude (A) and phase (B) error of the digital control system with an integral controller in the phase loop.

specification given in Table I. The relative amplitude could be stabilized to about 2.5×10^{-4} (rms). This error exceeds the specification by a factor of approximately 3 but is still an improvement when compared to the old system (by a factor of 8). Nevertheless, further improvements of the control algorithm are necessary to increase the amplitude stability. Furthermore the long-time stability of the system needs to be tested. Finally, the behavior of the new rf control system judged from the operational view was easy and convenient.

To complete the performance check, the temperature drifts of the rf board as a whole was measured in the rather extreme range from 10°C to 40°C . Within this range, the amplitude reading of a constant rf source changed by 1.5% while the phase varied by approximately 3° which is within the specifications of the rf components. At an envisaged operating temperature of 25°C , the slopes are $5 \times 10^{-4}/\text{K}$ for the amplitude and $0.07^\circ/\text{K}$ for the phase.

To meet the requirements (see Table I) especially for the amplitude accuracy, several measures were taken: The rf board will be installed into a temperature controlled frame being placed inside a water cooled rack. The expected temperature variation of the rf board is 1°C . In addition, a temperature sensor is placed on the rf board adjacent to the amplitude detector which can be read out by the FPGA

board; also the current algorithm does not make use of this. Based on the operational experience this is subject for further improvements.

Moreover, the long term stability of the accelerator against drifts is controlled by a feedback system, which continuously measures the beam energy via a time of flight measurement [11]. This system has a measured resolution of 7×10^{-5} (in energy) and will adjust directly the amplitude settings of the rf control loops in the near future.

V. CONCLUSIONS

For future operation of the S-DALINAC a new, digital rf control system has been designed, built, and a prototype has been tested. In contrast to similar systems, the 3 GHz high frequency signals are converted down to the baseband inside the rf board. The low frequency signals are transferred to the FPGA board, where the signal processing is done. The measured performance of the new system including a modified algorithm exceeded that of the existing control loops. Concluding, the digital control system is ready to replace the old control loops. As a first step, the upgraded injector linac [12] will be operated with the new system soon. Further improvements of the amplitude stability are necessary but can be done in parallel to the operation of the new digital system by working on the algorithm being programmed into the FPGA.

The new rf control system was designed with a physical interface between the rf and the FPGA board. Both parts are connected via a plug connector with a defined pin assignment. This modularity allows adapting different operating frequencies by replacing the rf and not the FPGA module. With a minimum effort it was possible to design a 1.3 GHz rf module by simply changing the directional couplers on the board. Currently, a 324 MHz and a 6 GHz version are under design. In principle, all frequencies in-between seem to be possible—the necessary redesign efforts (strictly limited to the rf module) are expected to be reasonable small.

ACKNOWLEDGMENTS

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