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# Defects in Cd\_{3}As\_{2} epilayers via molecular beam epitaxy and strategies for reducing them

A. D. Rice, K. Park, E. T. Hughes, K. Mukherjee, and K. Alberi Phys. Rev. Materials **3**, 121201 — Published 9 December 2019 DOI: 10.1103/PhysRevMaterials.3.121201 Defects in Cd<sub>3</sub>As<sub>2</sub> Epilayers Via Molecular Beam Epitaxy and Strategies for Reducing Them

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# Abstract

Molecular beam epitaxy offers an exciting avenue for investigating the behavior of topological semimetal  $Cd_3As_2$ , by providing routes for doping, alloying, strain engineering, and heterostructure formation. To date, however, minimal exploration has been devoted to the impact of defects that are incorporated into epilayers due to constraints imposed by the substrate and narrow growth window. Here, we use a combination of lattice-matched  $Zn_xCd_{1-x}Te$  buffer layers, miscut substrates and broadband illumination to study how dislocations, twins and point defects influence the electron mobility of  $Cd_3As_2$ . A combination of defect suppression approaches produces  $Cd_3As_2$  epilayers with electron mobilities upwards of 15,000 cm<sup>2</sup>/V-s at room temperature.

## I. Introduction

Topological semimetals provide rich systems in which to explore new and interesting physics [1,2]. Their symmetry-protected band touching nodes with linear dispersions can host relativistic massless electrons at the Fermi level and support an array of transport behaviors not typically observed in trivial semiconductors or metals. Recent experimental investigations in Dirac and Weyl semimetals have demonstrated evidence for Fermi arcs [3], the quantum Hall effect [4], and giant magnetoresistance [5]. These breakthroughs will undoubtedly form the basis for future technologies, such as low-dissipation electronics and novel spintronics [6].

In parallel to these discovery efforts, it is critically important to develop the topological semimetal materials themselves. High quality crystals in bulk, epitaxial layer and nanostructure forms are necessary to enable future progress on both scientific and technological fronts. The Dirac semimetal Cd<sub>3</sub>As<sub>2</sub> is a primary example [7]. Although many of the initial bandstructure and transport physics have been carried out in bulk single crystals [5,8], synthesis in epitaxial layers allows us to study the roles of confinement, strain[9], and heterostructures on their properties as well as fabricate them into devices.

Two factors strongly influence epitaxial growth of  $Cd_3As_2$  and its resulting properties. The first is the substrate.  $Cd_3As_2$  has a tetragonal crystal structure at temperatures < 475 °C with a  $I4_1/acd$  space group and lattice parameters a = 1.263 nm and c = 2.543 nm [10]. The atomic arrangement of its preferred (112) growth plane mirrors that of the (111) plane of zinc blende crystals [11]. Coincident atomic arrangements between the two can be achieved when the lattice constant of the zinc blende crystal is between those of ZnTe and CdTe. Previous growth on GaSb and CdTe substrates indicates that careful control of extended defects is necessary to achieve high electron mobilities [11,12]. Additionally, II-VI alloy substrates offer advantages over III-Vs due to their higher bandgaps, which limit them from

\*Author to whom correspondence should be addressed: Anthony.rice@nrel.gov introducing parallel conduction channels. The second factor influencing epitaxy is the relatively narrow window of growth parameters that can be accessed. The high vapor pressure of  $Cd_3As_2$  in vacuum practically restricts growth to temperatures below 250 °C, limiting the grower's ability to control surface morphology and defect formation. Even lower temperatures << 200 °C are necessary to maintain reasonable growth rates without loss to re-evaporation. In this context, approaches are needed to reduce point and extended defects generated as a result of heteroepitaxy or the use of low growth temperatures to realize high quality epitaxial structures that will enable future scientific and technological advances.

Here, we present a framework for  $Cd_3As_2$  growth by molecular beam epitaxy (MBE) using elemental sources and lattice-engineered II-VI buffer structures. Relaxed  $Zn_{1-x}Cd_xTe$  buffer layers on miscut GaAs(111) substrates spanning the entire solid solution provide a platform to control extended defects and strain conditions. Growth of  $Cd_3As_2$  from elemental sources, allowing for flexibility in stoichiometry and defect control, is then demonstrated on these buffer structures. Finally, broadband light stimulation is explored as a route to further improve the electron mobility in  $Cd_3As_2$  epilayers while maintaining low substrate temperatures. This study systematically explores the impact of each approach on the electron mobility as well as the interplay between them. We find that the combination of all three approaches ultimately improves the electron mobility and maximizes flexibility in designing the growth conditions of  $Cd_3As_2$  epilayers, alloys and heterostructures for a variety of investigations.

## II. Experimental Methods

Epilayers were grown in an interconnected, dual chamber Omicron EVO25 MBE system. All group II, III and VI sources were evaporated from effusion cells, while As<sub>4</sub> was evaporated from cracker sources in both chambers. Substrate temperatures were calibrated using a k-space band-edge thermometry system. Oxide removal of GaAs(111) under As<sub>4</sub> was performed in a dedicated III-V chamber followed by growth of a 300-nm GaAs buffer layer at high temperatures (>610°C) and low V/III ratios (3-5:1) [13]. The substrates were then cooled down and capped with an arsenic film. Samples were subsequently removed from vacuum and re-loaded on Mo blocks specific to the II-VI chamber to minimize contamination. The arsenic cap was thermally desorbed at ~350 °C, and the substrate was cooled down to commence II-VI and II-V growths. Specific growth conditions are described below. Unless noted, the sample surface was illuminated with broadband light from a Xe lamp (Oriel 6255) during growth of both the II-V buffer and Cd<sub>3</sub>As<sub>2</sub> epilayers. The lamp powers are stated below. Hall measurements were performed at room temperature using annealed indium contacts and Van der Pauw geometry under excitation voltages of 5 mV (50-200  $\mu$ A). Multiple samples were measured for each growth condition to produce the mobility ranges reported in the results section. Electron-channeling contrast imaging (ECCI) was used to probe for structural defects in the Cd<sub>3</sub>As<sub>2</sub> epilaylers [14]. Images were taken in the Cd<sub>3</sub>As<sub>2</sub> (-408)/(-440) channeling condition to characterize threading dislocation defect populations and other extended defects.

### III. Results

We first discuss the properties of the lattice-engineered II-VI buffer layers, as they will affect the  $Cd_3As_2$  morphology and electron mobility. Figure 1 shows x-ray diffraction (XRD) scans, reflective high energy electron diffraction (RHEED) patterns and atomic force microscopy (AFM) scans from typical buffer structures. All buffers started with a ZnTe epilayer (7.3% mismatch with GaAs), grown directly on on-axis



**Figure 1**.(a) XRD of  $Zn_xCd_{1-x}Te/ZnTe/GaAs$  buffer structures as well as an unstrained  $Cd_3As_2$  epilayer. Dotted lines correspond to expected lattice parameters. (b-e) AFM and RHEED images of a subset of surfaces in the  $Cd_3As_2/Zn_xCd_{1-x}Te/GaAs$  structure. All GaAs substrate orientations were on-axis.

GaAs(111) using a Zn treatment prior to growth to maximize the ZnTe crystalline quality [15]. Growth using a VI/II ratio of 2:1 (total absolute beam flux of  $3*10^{-7}$  Torr), a substrate temperature of 330 °C and broadband illumination at a lamp power of 100 W produced the smoothest films and highest intensity thickness fringes in XRD (Fig. 1a), consistent with sharp interfaces. Stoichiometric or group II rich growths resulted in very spotty RHEED patterns (not shown). Growing these epilayers thicker than 25 nm was also found to result in rougher morphologies. After ZnTe, a final Zn<sub>x</sub>Cd<sub>1-x</sub>Te epilayer was grown. For the extreme endpoint of CdTe, an approximately 150 nm layer was grown on the relaxed ZnTe surface under similar flux conditions at a lower substrate temperature (~240 °C), resulting in film roughnesses comparable to the starting GaAs layers. Zn<sub>x</sub>Cd<sub>1-x</sub>Te epilayers of mixed composition were grown at intermediate temperatures depending upon the relative Zn and Cd content. For instance, a Cd/Zn beam flux ratio of ~2:1 and a substrate temperature of 290 °C were used to achieve a lattice matching composition (Zn<sub>0.42</sub>Cd<sub>0.58</sub>Te) to the Cd<sub>3</sub>As<sub>2</sub> epilayer.

We next discuss the properties of the  $Cd_3As_2$  epilayers grown on these II-VI buffers. Table I summarizes the impact of the buffer composition, substrate miscut and broadband illumination on the  $Cd_3As_2$ electron mobility.  $Cd_3As_2$  growth was performed at substrate temperatures of approximately 100-120 °C under  $As_4$  rich conditions and combined absolute fluxes of 5-8\*10<sup>-7</sup> Torr. These low temperatures are required due to the high vapor pressure of  $Cd_3As_2$  [16]. Slightly higher substrate temperatures were previously found to produce higher electron mobilities, where a nearly two-fold increase was observed when raising the temperature from 140 °C to 210 °C [111]. However, these temperatures also require high flux rates to overcome elevated  $Cd_3As_2$  decomposition, so we therefore utilized much lower temperatures that are more practical for growth. All growths under illumination conditions were carried out with a Xe lamp setting of 100 W except in the power-dependence study discussed later. Figure 1e shows RHEED and AFM results from Cd<sub>3</sub>As<sub>2</sub> epilayers grown on a lattice-mismatched CdTe-terminated buffer on an on-axis GaAs substrate. CdTe layers showed smoother morphologies and narrower diffraction peaks than ZnTe and also allows for comparison with previous reports [11,17]. A 4x reconstruction is observed parallel to the [0-11] and [-211] directions (relative to GaAs(111)). A smooth transition between the II-VI and Cd<sub>3</sub>As<sub>2</sub> is observed, with no evidence of roughening during film nucleation. Previous reports have not discussed the surface reconstruction explicitly, but published images appear to show faint 4x streaks [11,17]. The lattice parameters of unstrained Cd<sub>3</sub>As<sub>2</sub> epilayers on lattice-matched Zn<sub>x</sub>Cd<sub>1-x</sub>Te buffers, as measured by XRD (Fig. 1a) are in good agreement with reported values, as shown in Fig. 1a on a lattice matched buffer layer, while AFM revealed 2D but rough morphologies relative to the underlying layers (~2-3 nm r.m.s. roughness). Epilayer thicknesses were not directly measured, but x-ray reflectivity performed on thinner samples suggest the Cd<sub>3</sub>As<sub>2</sub> epilayers presented



Figure 2. Phi scans of Cd3As2 (44<u>16</u>) peaks grown on  $Zn_xCd_{1-x}Te/ZnTe$  buffers with and without a substrate offcut.

here were approximately 200-250 nm thick. Baseline  $Cd_3As_2$  epilayers grown under dark conditions on on-axis substrates with lattice-mismatched CdTe buffers exhibit low electron mobilities ~2,000-4,000 cm<sup>2</sup>/V-s. The electron mobilities improved to 4,000-5,000 cm<sup>2</sup>/V-s when broadband illumination was applied. All films, regardless of the illumination conditions, had sheet carrier concentrations of 3-6E13 cm<sup>-2</sup>, which corresponds to 1-3E18 cm<sup>-3</sup> given the approximate film thicknesses.

Previous reports showed mild twinning arising at the  $Cd_3As_2$  interface [12, 11]. Twinning is also a known issue in CdTe epilayers [18]. Figure 2 displays phi scans of the (44<u>16</u>) peaks of Cd<sub>3</sub>As<sub>2</sub> grown on Zn<sub>x</sub>Cd<sub>1-x</sub>Te buffers. The six-fold symmetry of these peaks arises from the 180° rotations that occur during twinning. Similar degrees of twinning are observed in both Cd<sub>3</sub>As<sub>2</sub> layers (red curve) and Zn<sub>x</sub>Cd<sub>1-x</sub>Te layers across the entire solid solution grown on on-axis substrates (not shown), suggesting twinning is largely initiated in the buffer layers and then propagates throughout the structure. Twinning was substantially reduced by

Growth Condition			Electron Mobility [cm2/V-s]
Substrate Miscut	II-VI Buffer	Illumination	
On axis	CdTe	Dark	2,000-4000
On axis	CdTe	Illuminated	4,000-5,000
On axis	Zn <sub>0.42</sub> Cd <sub>0.58</sub> Te	Illuminated	4,500-6,000
3° miscut	CdTe or ZnTe	Illuminated	7,000-9,000
3° miscut	Zn <sub>0.42</sub> Cd <sub>0.58</sub> Te	Dark	7,000-8,000
3° miscut	Zn <sub>0.42</sub> Cd <sub>0.58</sub> Te	Illuminated	13,000-15,000

Table I. Summary of Cd<sub>3</sub>As<sub>2</sub> electron mobility based on substrate, buffer, and growth conditions



**Figure 3**. (a-c) Reciprocal space maps and (d-i) ECCI images of  $Cd_3As_2$  grown on ZnTe,  $Zn_{0.42}Cd_{0.58}Te$ , and CdTe buffer structures. Electron mobility and sheet density density from room temperature Hall measurements are noted in the middle panels. Measured TDD from the ECCI images are noted in the bottom panels.

performing growths under similar conditions on wafers 3° mis-cut toward (2-1-1), as shown in Fig. 2, similar to previous reports [12]. In particular, little evidence of twins (1% or less) was observed in both the  $Cd_3As_2$  (blue curve) or  $Zn_{0.42}Cd_{0.58}$ Te layers (not shown) with nearly lattice-matched compositions.

Figure 3 summarizes the impact of the II-VI buffer lattice constant on the Cd<sub>3</sub>As<sub>2</sub> properties. Reciprocal space maps (Figs. 3(a-c)) confirm that the Cd<sub>3</sub>As<sub>2</sub> epilayers are highly relaxed on 3° miscut CdTe (2.3% mismatch) and ZnTe (-3.4% mismatch) buffers, while Cd<sub>3</sub>As<sub>2</sub> grown on Zn<sub>0.42</sub>Cd<sub>0.58</sub>Te buffers appeared nearly lattice matched with narrower peak shapes. No significant mobility difference is observed between epilayers grown on either ZnTe and CdTe buffers (Figs. 3d and 3f), despite the lower Cd<sub>3</sub>As<sub>2</sub> surface roughness on CdTe. This suggests that morphology only plays a minor role in limiting the electron mobility compared to other defects, which is consistent with previous reports [11].

To evaluate the influence of the II-VI buffer lattice constant on extended defects in  $Cd_3As_2$ , we performed ECCI measurements on  $Cd_3As_2$  epilayers grown on all three buffers. The micrographs (Fig. 3(d-i)) indicate that the epilayers have similar threading dislocation densities (TDD) of ~4-8 x 10<sup>8</sup> cm<sup>-2</sup>; however, there appears to be a substantial reduction in the density of other extended defects in the epilayers grown on lattice-matched  $Zn_xCd_{1-x}Te$  buffers compared to those grown on lattice-mismatched ZnTe and CdTe buffers. Figure 4 highlights the two major differences observed in unstrained and relaxed  $Cd_3As_2$ . The former is more structurally homogeneous but does show signs of pitting at the film surface, as seen in the AFM micrograph presented in Fig. 4a. The later shows regions of structural defects, such as the boundary highlighted in Fig. 4b. These types of defective regions are only observed in relaxed





Cd<sub>3</sub>As<sub>2</sub> films. Although we are still exploring the origin of these differences, removing the lattice mismatch between the buffer and epilayer appears to help suppress the formation of certain types of extended defects.

Suppression of extended defects has a substantial effect on the electron mobility. When twinning is reduced through the use of a miscut substrate but a lattice-mismatched CdTe or ZnTe buffer is used, the electron mobility improves to 7,000-9000 cm<sup>2</sup>/V-s. The addition of a lattice-matched  $Zn_{0.42}Cd_{0.58}$ Te buffer further increases the mobility to 13,000-15,000 cm<sup>2</sup>/V-s. These values are close to the highest reported room temperature values for epitaxially grown thin films (19,300 cm<sup>2</sup>/V-s [11]).

Given the previous success broadband illumination of the growth surface has had on improving the optical properties of II-VI semiconductors grown at low temperature [19], we explore it as a tool for further improving epitaxial Cd<sub>3</sub>As<sub>2</sub>. All epilayers discussed up to this point were grown under broadband illumination with 100 W power. Figure 5 details the impact of Xe lamp power on the electron mobility and surface morphology of Cd<sub>3</sub>As<sub>2</sub> epilayers grown on lattice-matched, miscut Zn<sub>0.42</sub>Cd<sub>0.58</sub>Te buffers. While the film morphology became rougher with increasing illumination, the electron mobility increased up to intermediate lamp powers of 100 W. Illumination of semiconductor surfaces during growth has been demonstrated to reduce point defects, which is likely a particular concern here due to the low substrate temperatures used for Cd<sub>3</sub>As<sub>2</sub> growth. Light has previously been found to affect semiconductor growth by increasing adatom desorption [20], altering surface kinetics [21] and modifying defect formation [22]. Changes in surface kinetics under illumination could also be

responsible for the surface roughening [23]. Both Cd and As have non-unity sticking coefficients, so it is possible the net result of illumination on this surface is more Cd and/or As desorption. Reduction in defects by light stimulation would cause an increase in the electron mobility, although the exact pathways and the specific defect population affected have not been identified at this time. Further investigation is required to understand the underlying mechanisms of both trends in this material system. However, we reiterate the point that broadband light stimulation is found to be a key method for producing room temperature electron mobilities > 13,000 cm<sup>2</sup>/Vs at growth temperatures below 170 °C.

While improvements in Cd<sub>3</sub>As<sub>2</sub> electron mobility were gained through the use of lattice-matched II-VI buffers, miscut substrates, or broadband illumination, only a combination of the three produced electron mobilities above 10,000 cm<sup>2</sup>/V-s. Consistent with Matthiessen's rule, our results illustrate that reducing the density of one type of defect can only improve the electron mobility of Cd<sub>3</sub>As<sub>2</sub> so much when relatively large densities of others exist. For example, this rule is evident in the magnitude of the improvement produced by broadband light illumination. When growth is carried out on on-axis substrates and lattice-mismatched buffers, illumination only increased the electron mobility by ~1,000 cm<sup>2</sup>/V-s, suggesting the mobility is dominated by extended defects. However, when illumination was applied to growth on miscut substrates and lattice-matched Zn<sub>0.42</sub>Cd<sub>0.58</sub>Te buffers, illumination produced a 5,000 cm<sup>2</sup>/V-s increase. This result suggests that illumination affects some additional type of defect population beyond dislocations and twin defects. On the whole, the systematic comparison of growth conditions, defect types and the resulting electron mobility and which ones must be targeted to realize improvements.

Our study indicates that multiple types of defects are also the main cause of the low electron mobilities



**Figure 5.** AFM images and measured room temperature electron mobilities and r.m.s. roughnesses of  $Cd_3As_2$  films under (a) 0 W, (b) 20W, (c) 100W, and (d) 150W UV lamp illumination. Values correspond to UV lamp power.

in epitaxially-grown  $Cd_3As_2$  compared to high quality bulk single crystals (42,850 cm<sup>2</sup>/V-s [24]). We suggest the following strategies to realize further gains. The dislocation densities in our  $Cd_3As_2$  epilayers (~10<sup>8</sup> cm<sup>-2</sup>) are still quite high and will need to be reduced through better design of the II-VI buffers. Disorder and point defects can be reduced through annealing above the practical growth temperatures used here with a sufficiently stable capping layer [25]. The role of the II/V ratio must also be explored to obtain additional insight into the role of Cd or As vacancies (and other native defects) on the electron mobilities. However, the higher symmetry of the zinc blende structure will ultimately be a limiting factor at some point.

### IV. Conclusions

In summary, we demonstrate a II-VI platform providing tunable lattice constants and smooth morphologies for Cd<sub>3</sub>As<sub>2</sub> growth. Controlling defects using miscut substrates, lattice-matched buffer layers and broadband illumination produced higher electron mobilities while maintaining lower growth temperatures to limit Cd<sub>3</sub>As<sub>2</sub> decomposition. Our results provide insight into the types of defects formed within epitaxial Cd<sub>3</sub>As<sub>2</sub> and their influence on the transport properties. Such studies are needed as we push the limits of epitaxial crystal quality to enable new physics discoveries within the Cd<sub>3</sub>As<sub>2</sub> material system and utilize it for future technological advances.

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