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Effects of surface tunneling of two-dimensional hole gases in undoped Ge/GeSi heterostructures

Yi-Hsin Su, Yen Chuang, Chia-You Liu, and Jiun-Yun Li*

Graduate Institute of Electronic Engineering, National Taiwan University, Taipei 10617, Taiwan

Tzu-Ming Lu

Sandia National Laboratories, Albuquerque, New Mexico 87185, USA

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We investigate the effect of surface tunneling on charge distributions of two-dimensional hole gases (2DHGs) in undoped Ge/GeSi heterostructures. As in the electron channel case, the 2DHG density saturates at a high gate voltage. As the channel depth of 2DHG increases, a crossover of charge distributions in the system from equilibrium to non-equilibrium is observed at a depth of ~ 50 nm. A surface tunneling model is proposed to explain the density crossover. Magneto-transport analysis is performed to investigate the limiting scattering mechanisms. The power law dependence of mobility on density suggests that the dominant scattering mechanisms for the shallow- and deep-channel 2DHGs are remote impurity and background impurity scattering, respectively. Clear quantum Hall plateaus and vanishing longitudinal magneto-resistance are observed in the 2DHG device of channel as shallow as 9 nm.

I. INTRODUCTION

Germanium is considered a promising channel material for replacing silicon in continuing complementary metaloxide-semiconductor (CMOS) scaling due to its high hole mobility at room temperature¹-³. Compressive strain in Ge further enhances the hole mobility up to $4.500 \text{ cm}^2/\text{Vs}$ by formation of a two-dimensional hole gas (2DHG) in a Ge/GeSi heterostructure⁴. Due to the development of relaxed Ge epitaxy on Si substrates in the past decade, a record high mobility in a Ge 2DHG over 1 million was demonstrated at 12 K^5 . Most prior work has focused on modulation-doped structures $^{6}-^{8}$, where the carrier density is modulated by varying the concentration of remote dopants and the distance between the 2DHG and the doping layer. An alternative device architecture is the undoped heterostructure field-effect transistors⁹¹⁰. Not only was the highest two-dimensional electron gas (2DEG) mobility achieved in an undoped structure¹¹, but spin manipulation was also demonstrated by several groups⁹¹²¹³. An extremely low electron density down to $\sim 1 \times 10^{10} \text{ cm}^{-2}$ was achieved by top gating in undoped structures¹⁴. On the high density end, the density can be modulated to an upper limit by gating, which was higher than the expected values at equilibrium and can be attributed to non-equilibrium in charge distributions by surface tunneling¹⁵. In the surface tunneling model, maximum electron density by gating is independent of the 2DEG depth, but only determined by the conduction band offset at the Si/SiGe heterojunction. An enhanced mobility was also reported and attributed to the passivated surface impurities by the tunneled carriers¹⁶. For gated devices such as quantum dots, surface tunneling could lead to parallel conduction in the surface channel¹⁶, resulting in ineffective gating. On the other hand, very few studies on Ge 2DHGs formed in undoped Ge/GeSi heterostructures have been reported 1017 . As a potential platform for quantum devices with high mobility and integrability with Si, undoped Ge/GeSi heterostructures are urging for more investigations. Whether the surface tunneling effect is universal in 2D systems or relevant to certain surface effects in Si 2DEGs also remains unanswered.

In this work, we investigate the effect of surface tunneling on electrostatics in Ge/GeSi heterostructures by varying the 2DHG depth, denoted as t. Similar to prior work on 2DEGs, an upper limit of carrier density exists for all channel depths, which confirms the universality of surface tunneling for undoped structures. For devices with t < 50 nm, the carrier density agrees with Poisson's equation, while for devices with t > 50 nm, the carrier density is much greater than the equilibrium value. This density crossover of equilibrium and nonequilibrium charge distributions in 2DHGs can be attributed to surface tunneling. Furthermore, we show that the effective gate capacitance is much reduced for the shallow-channel devices, which can also be explained by surface tunneling. To identify the limiting scattering mechanisms in undoped Ge/GeSi heterostructures, we performed magneto-resistance measurements. The power law dependence of mobility on density and Dingle ratio analysis indicate that remote impurities at the oxide interface are the limiting scattering sources for shallowchannel devices. For deep-channel devices, the mobility is limited by background impurities or other defects such as dislocations. The article is organized as follows: In section II, we will introduce the experiment including the epitaxy, fabrication, and measurement. In section III and IV, effects of surface tunneling on 2DHG density and gate efficiency will be discussed, respectively. In section V, magnetotransport measurements are discussed. Finally, we will summarize our work in section VI.

II. TWO-DIMENSIONAL HOLE GASES IN GERMANIUM SILICON HETEROSTRUCTURES

Undoped Ge/Ge_{0.85}Si_{0.15} heterostrutures were epitaxially grown on Si (001) substrates by reduced pressure chemical vapor deposition with GeH_4 and SiH_4 as the precursors. Fig. 1(a) shows a schematic of an undoped Ge/GeSi heterostrucre. First, a Si buffer layer of 200 nm was deposited at 850 °C, followed by low-temperature deposition of a thin relaxed Ge layer of 200 nm to serve as a virtual substrate. High-temperature annealing at 825 °C was performed for 10 minutes to reduce dislocations induced by the large lattice mismatch between Si and Ge^{18} . A Ge buffer layer of 100 nm was then deposited followed by a constant $Ge_{0.85}Si_{0.15}$ relaxed buffer layer of 3 μ m, both at 450 °C. A strained Ge layer of 25 nm, where the 2DHG resides, was grown with a $Ge_{0.85}Si_{0.15}$ cap layer as a top barrier to separate the 2DHG and the surface. Four Ge/GeSi heterostructures of different 2DHG depths (t = 9, 26, 58, and 116 nm) were grown to investigate the density crossover and scattering mechanisms in the Ge 2DHG system. The thicknesses of epitaxial layers were determined by secondary ion mass spectrometry (SIMS) and cross-sectional transmission elec-



FIG. 1. (a) Schematic and (b) A XTEM image of undoped Ge/GeSi heterostructures with t = 26 nm (c) Hole density vs. gate voltage for 2DHG devices with t = 9 nm (orange), 26 nm (red), 58 nm (blue), and 116 nm (purple). Inset: zoom-in of the curves for the devices with t = 58 nm (blue) and 116 nm (purple)

tron microscopy (XTEM). Fig. 1(b) shows the XTEM image of an undoped Ge/GeSi heterostrucre with t = 26 nm. The compositions of Si and Ge and impurities are characterized by SIMS. The strain distributions within the Ge/GeSi heterostructures were investigated by reciprocal space mapping, which confirmed that the Ge layers are fully strained.

Enhancement-mode Hall-bar devices with a top gate to modulate the 2DHG density were fabricated by photolithography. First, 250 nm of aluminum was deposited by e-beam evaporation with a post-annealing step at 490 °C for 30 s to form Ohmic contacts. 90 nm of Al₂O₃ was deposited by atomic layer deposition at 200 °C followed by a Ti/Au (10 nm/150 nm) gate stack by e-beam evaporation. The devices were measured at 300 mK in a ³He cryogenic system using standard low frequency lockin techniques with a low excitation current (~10 nA). The hole density was modulated by top gating and the associated mobility was determined from the zero-field longitudinal magneto-resistance (R_{xx}) and the slope of low-field Hall resistance (R_{xy}) vs. magnetic field.

III. THE EFFECT OF SURFACE TUNNELING ON 2DHG DENSITY

The gate voltage dependence of hole density is plotted in Fig. 1(c). There are two regimes of hole population in all devices. At small gate biases, the hole density increases linearly as the gate voltage sweeps more negative, consistent with the parallel-plate capacitor model. At large gate biases, the hole density saturates for all devices. For deep-channel devices (t = 58 nm and 116)nm), the saturation densities are the same ($\sim 1.8 \ge 10^{11}$ cm^{-2}) [inset of Fig. 1(c)]. For shallow-channel devices. the densities are different and higher than that for the deep-channel devices ($\sim 8 \ge 10^{11} \text{ cm}^{-2}$ and $\sim 3.8 \ge 10^{11}$ cm^{-2} for devices of t = 9 nm and 26 nm, respectively). Density saturation was previously reported in a Si/SiGe 2DEG system with an upper limit due to the tunneling of 2D carriers to the surface, leading to a non-equilibrium state of charge distributions in the system¹⁵. The saturation densities were the same for all devices of different channel depths in Ref. 15. However, in our work, the same saturation densities could only be observed for the deep-channel devices, but not the shallow-channel devices.

To investigate the discrepancy, we calculated the saturation (maximum) hole density by Poisson's equation and compared to the experimental results, as shown in Fig. 2(a)¹⁹. Square points represent the experimental data and the solid line represent the calculated results. The maximum of hole density in the 2DHG channel occurs when the Fermi level aligns with the valence band edge at the Al₂O₃/GeSi interface, as shown in Fig. 2(b). When the valence band edge is pulled up to cross the Fermi level by further increasing the gate voltage, the holes start to populate in the surface channel, which



FIG. 2. (a) Saturation density (p_{max}) vs. 2DHG depth and (b) band diagram of Ge/GeSi heterostructure and its charge distribution in the regime of density saturation.

prevents further hole accumulation in the buried quantum well. While a Schrödinger-Poisson solver provides a quantum correction to the classical results, for simplicity, we used Poisson's equation to qualitatively explain our data. According to Poisson's equation, the saturation density (p_{max}) is $\Delta E_v \epsilon_0 \epsilon_r / e^2 t^{15}$, where ΔE_v is the valence-band offset at the Ge/GeSi heterointerface, ϵ_0 is the vacuum permittivity, ϵ_r is the relative permittivity of the GeSi barrier layer, and e is the electron charge. The band-offset ΔE_v between Ge and Ge_{0.85}Si_{0.15} is estimated to be 110 meV²⁰. The relative permittivity ϵ_r of $Ge_{0.85}Si_{0.15}$ is estimated to be 15.6, interpolated by the values of Si (11.7) and Ge (16.3). By comparing our experimental data to the calculations, it is apparent that a crossover from equilibrium to non-equilibrium in 2D carrier density exists at a channel depth of ~ 50 nm. For t < 50 nm, the experimental data and the calculated equilibrium densities by Poisson's equation match very well, indicating that the charge distributions in the system are in the equilibrium state. On the other hand, for the deep-channel devices (t > 50 nm), the density (dashed line) is higher than the calculated value.

To reach the equilibrium state for a Ge 2DHG, holes must accumulate at the surface. When the valence band edge of the surface quantum well crosses the Fermi-level, there are three possible ways for holes to reach the surface: thermal generation, injection from the source/drain electrodes, or tunneling from the buried quantum well. Thermal generation is unlikely to occur since the measurements were carried out at 0.3 K. Injection from the electrodes is also highly suppressed due to the poor $Al_2O_3/GeSi$ interface²¹. Interface traps and disorder strongly localize the injected carriers, prohibiting lateral transport at the surface between electrodes. Hence, we believe that holes have to be injected from the electrodes to the buried quantum well first, and then tunnel to the surface layer, as Ref. 15 suggested. At a small gate bias, the electric field is small and the tunneling probability is low. The time scale of the density change in the surface quantum well via surface tunneling could be too long for a density change to be detectable during the measurements¹⁵.

By Gauss's law, the added carriers with an increasing

gate voltage can only enter the 2DHG channel first for charge conservation¹⁶. The hole density in the buried channel will increase with gate voltage beyond the equilibrium density. As the electric field increases with the gate voltage, the tunneling barrier becomes smaller, leading to a non-negligible tunneling current. As a result, a loss of 2DHG carriers to the surface is expected, which in turn reduces the electric field. Further gate voltage increase would induce the carriers into the buried channel, and the electric field would increase again. A balance is then established, resulting in a constant electric field and an upper limit in carrier density in the buried channel¹⁵.

For the shallow channel devices, the saturation densities are much higher than the observed upper limit for the deep-channel devices. The saturation densities for shallow-channel devices match the calculation results very well, suggesting that the shallow-channel devices were in equilibrium. We believe that the density crossover between equilibrium and non-equilibrium in 2DHG is due to the occurrence of surface tunneling. The band diagrams of Ge/GeSi heterostructures of t = 80 nmand 26 nm are illustrated in Fig. 3(a) and (b), respectively, both biased to accommodate holes of the same density at the same upper limit. For the deep-channel devices (t = 80 nm), the carriers in the Ge quantum well could tunnel to the surface triangular quantum well, leading to a non-equilibrium state [Fig. 3(a)]. Meanwhile, for the shallow-channel devices at the same saturation density, the associated band diagram shows that a misalignment between the buried quantum well and the surface quantum well prohibits surface tunneling [Fig. 3(b)]. As a result, carrier loss would not occur via surface tunneling. As the gate bias increases, the valence band edge would be pulled up further such that 2DHG can now "see" the available energy states in the surface quantum well, allowing fast tunneling to take place [Fig. 3(c)]. Since the distance between the buried channel and the surface layer is short for the shallow-channel devices, the tunneling rate is much higher than that for deep-channel devices. Thus, the tunneled carriers are enough to fill the vacant states below the Fermi level and the thermal equilibrium is reached.

IV. THE EFFECT OF SURFACE TUNNELING ON GATE EFFICIENCY

The effective gate capacitance can be extracted from the slope of the linear part of hole density vs. gate voltage (dash lines in Fig. 1(c)) As Fig. 4(a) shows, we found that the slopes for the deep-channel devices fit well with the theoretical calculation by assuming that the relative dielectric constants of Al₂O₃ and GeSi layers are 6.2 and 15.6, respectively. However, for the shallow-channel devices, unexpectedly low gate capacitance was observed (one sixth of the predicted values). We believe that this could also be attributed to surface tunneling. The band diagrams of both shallow-channel (t = 9 nm) and



FIG. 3. Band diagrams of (a) a deep-channel device (t = 80 nm) with a 2DHG density at the upper limit ($\sim 1.8 \times 10^{11} \text{ cm}^{-2}$) (b) a shallow-channel device (t = 26 nm) with the same 2DHG density as (a), and (c) with a 2DHG density beyond the upper limit ($\sim 3.8 \times 10^{11} \text{ cm}^{-2}$)



FIG. 4. (a) Effective gate capacitance vs. 2DHG depth. The experimental data points were extracted from the slopes of dashed lines in Fig. 1(c). (b) Band diagrams of shallow-channel device (t = 26 nm) and (c) deep-channel device (t = 116 nm) with defect states in the bandgap at the Al₂O₃/GeSi interface.

deep-channel (t = 58 nm) devices are shown in Fig. 4(b) and (c), respectively. There are high-density traps in the bandgap at the Al₂O₃/GeSi interface²¹. For the shallow-channel devices [Fig. 4(b)], the energy alignment of the subband in the buried quantum well with the interface states allows surface tunneling, resulting in loss of carriers in the buried quantum well and the reduction of effective capacitance. For the deep-channel devices [Fig. 4(c)], although the energy levels of subband and the interface traps are still aligned, the tunneling bar-



FIG. 5. Band diagrams of a shallow-channel device (t = 26 nm) capped with (a) a Ge layer (b) a Si layer.

rier is large enough to prohibit the holes in the quantum well from tunneling to the surface. Thus, holes remain in the quantum well with the effective capacitances equal to the series capacitance of the GeSi barrier and the Al_2O_3 layers.

The carrier loss in the quantum well via surface tunneling leads to an increase of trapped charges, at the surface (i.e. mobility is zero). While any charge (mobile or immobile) would contribute to the effective capacitance by the simple parallel-plate capacitance model, for Hall measurement, only carriers with non-zero mobilities in the buried quantum well (or the surface layer) can be measured. Thus, there is no contribution by those trapped charges in the surface states to the effective capacitance by Hall measurement. As a result, the effective capacitance is reduced for the shallow-channel devices.

To suppress tunneling, a heterostructure of a larger valence-band offset ΔE_V could be used to increase the tunneling barrier, which can be implemented by increasing the Si composition in the GeSi barrier. However, misfit dislocations induced by a larger lattice mismatch between the Ge active layer and the relaxed GeSi cap layer may further degrade the channel mobility. An alternative is to deposit a Ge cap layer on top of the heterostructures. The band diagram of Ge capped structure [Fig. 5(a)] shows that 2DHG cannot see any midgap states at the surface, prohibiting the tunneling even though the tunneling barrier is small. The effective capacitance of a Ge 2DHG device with a Ge cap layer will not be reduced since the hole subband energy in the Ge cap layer is much higher than that in the Ge QW layer, prohibiting the surface tunneling. Note that a Si cap layer, deposited in most of modulation-doped Si/SiGe or Ge/GeSi heterostructures, cannot prevent the surface tunneling in a Ge/GeSi heterostructure despite fewer defect traps in the Si/Al_2O_3 interface^{22_24} [Fig. 5(b)]. Thus, to block surface tunneling for effective gating, a Ge cap layer is required. However, for shallow-channel devices on undoped heterostructures, mobilities are much reduced due to stronger remote impurity scattering from the oxide interface. Furthermore, Ge/oxide interface is unstable compared to Si/oxide interface. The impact of Ge/highk interface on gating efficiency and 2DHG mobility is thus worth further investigation.

V. CARRIER TRANSPORT

Magnetotransport in Ge/GeSi heterostructures of different 2DHG depths was also investigated. The density dependence of Hall mobility is shown in Fig. 6. For each device, the mobility increases with density due to increased screening of charged impurities. A mobility decrease is observed with the decreasing 2DHG depth, due to the stronger remote scattering from the impurities at the oxide interface. A maximum mobility of $\sim 180,000$ cm^2/Vs is achieved for the device of t = 58 nm. A mobility up to $\sim 70,000 \text{ cm}^2/\text{Vs}$ is still obtained for the device of the shallowest channel (t = 9 nm), an indication of the high quality of the epitaxial growth and the oxide interface. To our surprise, the shallowest-channel can be turned on with such a high mobility, even with an inferior Al₂O₃/GeSi interface. For Si 2DEG devices, a thin Si cap layer is typically deposited to offer a better oxide interface than the SiGe barrier layer can offer. For Ge 2DHG devices, while a Si cap can be grown on top of the Ge-rich GeSi barrier layer, the large lattice mismatch and the required higher-temperature growth could lead to high-density dislocation defects²⁶. Alternative surface capping layers are necessary for a better oxide interface, to enhance hole mobility in a Ge/GeSi heterostructure of a shallow channel.

A Ge cap layer instead can be grown to prevent the above issue by Si growth. However, whether Ge or GeSi cap can offer a better surface has not been fully investigated yet²¹,²²-²⁴. Recently, Ge has become a promising channel material to replace Si for sub-7 nm CMOS technology and beyond . Some techniques to improve its oxide interface such as plasma-post oxidation²⁷, capped annealing²⁸, and ozone oxidation²⁹ have been demonstrated to be effective for the reduction of D_{it} (< 10^{12} cm⁻²eV⁻¹). We expect a combination of Ge cap layer with those surface treatments will be able to enhance the channel mobility by effective reduction of interface traps.

For the device of t = 116 nm, there is no further mobility increase, which implies the remote impurity scatter-



FIG. 6. Hole mobility vs. density for Ge/GeSi heterostructures of different 2DHG depths.



FIG. 7. Hall resistance (\mathbf{R}_{xy}) and longitudinal resistance (\mathbf{R}_{xx}) as a function of B field for Ge/GeSi heterostructures of $t = (\mathbf{a})$ 116 nm, (b) 58 nm, (c) 26 nm, and (d) 9 nm biased in the regime of density saturation. The numbers indicated in each figure are the filling factors (ν) of Landau levels

ing is no longer the dominant scattering mechanism. The power dependence of mobility on density ($\mu = n^{\alpha}$) shows that the remote impurity scattering dominates for the shallow-channel devices ($\alpha \sim 1.5$). For the deep-channel devices of t = 116 nm and 58 nm, α 's are 0.20 and 0.31, which suggests that the background impurity scattering or other mechanisms dominate³⁰.

Fig. 7 shows the magnetoresistance vs. magnetic field for Hall bar devices biased at the regime of density saturation. Quantum Hall plateaus in transverse resistance and concommitant vanishing longitudinal resistance are observed, showing the high quality of the epitaxial growth. Furthermore, a fractional quantum Hall state at the filling factor $\nu = 5/3$ is also observed for t =58 nm and 116 nm devices³¹³².

To extract the limiting scattering mechanisms for quantum transport, Dingle ratios $\alpha_D = \tau_t / \tau_q \sim \mu B_{SdH}$

TABLE I. Comparison of Dingle ratios for Ge 2DHGs and Si 2DEGs²⁵ at density saturation regime. Ge 2DEGs and Si 2DEGs with comparable depths are arranged as in the same row. The left three columns are for Ge 2DHGs and the right are for Si 2DEGs.

	Ge 2DHGs			Si 2DEGs	
Depth (nm)	Saturation Density (cm^{-2})	Dingle ratio	Depth (nm)	Saturation Density (cm^{-2})	Dingle ratio
9	$8.0 \ge 10^{11}$	3.5	10	$4 \ge 10^{11}$	1.3
26	$3.8 \ge 10^{11}$	4.7	25	$3 \ge 10^{11}$	9.4
58	$1.8 \ge 10^{11}$	9.6	48	$2 \ge 10^{11}$	81
116	$1.8 \ge 10^{11}$	8.5	100	$2 \ge 10^{11}$	125

were estimated (Table I), where τ_t and τ_q are transport and quantum lifetimes, and B_{SdH} is the magnetic field for the onset of SdH oscillations²⁵. The Dingle ratios are also compared with those of Si devices in Ref. 25. For shallow channel devices of Ge 2DHGs and Si 2DEGs, the Dingle ratios are small. This is expected due to the enhanced short-range Coulomb scattering from the remote impurities at the oxide/semiconductor interfaces. As the channel depth increases, the Dingle-ratio for Si 2DEGs increases by a factor of ~ 100 , suggesting that the background impurities have much less contributions to the short-range scattering rates. A mobility of $\sim 10^6$ $\rm cm^2/Vs$ was demonstrated for a Si 2DEG device of a deep channel, suggesting a low level of background impurities. On the other hand, the Dingle ratios are small for deepchannel Ge devices. This suggests that the background impurities be the dominant scattering sources.

VI. CONCLUSIONS

In summary, a crossover of equilibrium and nonequilibrium of 2DHG saturation density due to surface tunneling was reported. All devices showed density saturation at high gate biases. For the shallow-channel devices (t < 50 nm), the saturation density follows the prediction by Poisson's equation, and equilibrium in charge distributions in the system is established by fast surface tunneling. On the other hand, for the deep-channel devices (t > 50 nm), saturation densities are higher than the predicted equilibrium values and a constant saturation density (upper limit) was observed for different 2DHG depths. This surface tunneling also leads to ineffective gating with a reduction of gate capacitance for the shallow-channel devices by hole tunneling to the interface trap states. Effects of surface tunneling on Ge 2DHG electrostatics were investigated in depth and well explained by the surface tunneling model.

Magneto-resistance measurement was performed to characterize quantum transport of Ge 2DHGs. Remote impurity scattering is considered the dominant scattering mechanism for the shallow-channel devices, while for the deep-channel devices, the limiting scattering mechanisms could be background impurity scattering or other mechanism such as dislocations based on the analysis of power law dependence of mobility on density and Dingle ratios. Clear quantum Hall plateaus and a fractional quantum Hall state ($\nu = 5/3$) were clearly observed, an indication of high-quality epitaxial growth. The high mobility in the shallowest 2DHG achieved so far sheds light on the future of its quantum device applications.

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^{*} jiunyun@ntu.edu.tw; also at National Nano Device Laboratories, Hsin-Chu, Taiwan

¹ S. Madhavi, V. Venkataraman, and Y. H. Xie, Journal of Applied Physics 89, 2497 (2001).

² M. Myronov, K. Sawano, Y. Shiraki, T. Mouri, and K. M. Itoh, Applied Physics Letters **91**, 082108 (2007).

³ R. Pillarisetty, Nature **479**, 324 (2011).

⁴ М. Myronov, С. Morrison, J. Halpin, S. Rhead. J. Foronda. and D. Leadley, in 2014 7th International Silicon-Germanium Technology and Device Meeting (ISTDM) (Institute of Electrical and Electronics Engineers (IEEE), 2014).

- ⁵ A. Dobbie, M. Myronov, R. J. H. Morris, A. H. A. Hassan, M. J. Prest, V. A. Shah, E. H. C. Parker, T. E. Whall, and D. R. Leadley, Applied Physics Letters **101**, 172108 (2012).
- ⁶ B. Rössner, D. Chrastina, G. Isella, and H. von Knel, Applied Physics Letters 84, 3058 (2004).
- ⁷ K. Sawano, K. Toyama, R. Masutomi, T. Okamoto, N. Usami, K. Arimoto, K. Nakagawa, and Y. Shiraki, Applied Physics Letters **95**, 122109 (2009).
- ⁸ M. A. Zudov, O. A. Mironov, Q. A. Ebner, P. D. Martin, Q. Shi, and D. R. Leadley, Phys. Rev. B 89, 125401 (2014).
- ⁹ T. M. Lu, N. C. Bishop, T. Pluym, J. Means, P. G. Kotula, J. Cederberg, L. A. Tracy, J. Dominguez, M. P. Lilly, and M. S. Carroll, Applied Physics Letters **99**, 043101 (2011).
- ¹⁰ D. Laroche, S.-H. Huang, Y. Chuang, J.-Y. Li, C. W. Liu, and T. M. Lu, Applied Physics Letters 108, 233504 (2016).
- ¹¹ S.-H. Huang, T.-M. Lu, S.-C. Lu, C.-H. Lee, C. W. Liu, and D. C. Tsui, Applied Physics Letters **101**, 042111 (2012).
 ¹² B. M. Maune, M. G. Borselli, B. Huang, T. D. Ladd, P. W. Deelman, K. S. Holabird, A. A. Kiselev, I. Alvarado-Rodriguez,
- R. S. Ross, A. E. Schmitz, M. Sokolich, C. A. Watson, M. F. Gyure, and A. T. Hunter, Nature 481, 344 (2012).
- ¹³ K. Wang, C. Payette, Y. Dovzhenko, P. W. Deelman, and J. R. Petta, Phys. Rev. Lett. **111**, 046801 (2013).
- ¹⁴ T.-M. Lu, *High-Mobility Two-Dimensional Electrons in Si/SiGe Heterostructures: Realization and Transport Properties*, Ph.D. thesis, Princeton University (2011).
- ¹⁵ T. M. Lu, C.-H. Lee, S.-H. Huang, D. C. Tsui, and C. W. Liu, Applied Physics Letters **99**, 153510 (2011).
- ¹⁶ C.-T. Huang, J.-Y. Li, K. S. Chou, and J. C. Sturm, Applied Physics Letters **104**, 243510 (2014).
- ¹⁷ S. N. Holmes, P. J. Newton, J. Llandro, R. Mansell, C. H. W. Barnes, C. Morrison, and M. Myronov, Journal of Applied Physics **120**, 085702 (2016).
- ¹⁸ K. H. Lee, A. Jandl, Y. H. Tan, E. A. Fitzgerald, and C. S. Tan, AIP Advances **3**, 092123 (2013).
- ¹⁹ See Supplemental Material at [URL will be inserted by publisher] for calculations of the band diagrams from Fig .2-5.
- ²⁰ D. J. Paul, Semiconductor Science and Technology **19**, R75 (2004).
- ²¹ J.-H. Han, M. Takenaka, and S. Takagi, Journal of Applied Physics **120**, 125707 (2016).
- ²² L. Gomez, C. N. Chleirigh, P. Hashemi, and J. L. Hoyt, IEEE Electron Device Letters **31**, 782 (2010).
- ²³ R. Pillarisetty, B. Chu-Kung, S. Corcoran, G. Dewey, J. Kavalieros, H. Kennel, R. Kotlyar, V. Le, D. Lionberger, M. Metz, N. Mukherjee, J. Nah, W. Rachmady, M. Radosavljevic, U. Shah, S. Taft, H. Then, N. Zelick, and R. Chau, in 2010 International Electron Devices Meeting (Institute of Electrical and Electronics Engineers (IEEE), 2010).
- ²⁴ P. Goley and M. Hudait, Materials **7**, 2301 (2014).
- ²⁵ D. Laroche, S.-H. Huang, E. Nielsen, Y. Chuang, J.-Y. Li, C. W. Liu, and T. M. Lu, AIP Advances 5, 107106 (2015).
- ²⁶ B. Vincent, R. Loo, W. Vandervorst, J. Delmotte, B. Douhard, V. Valev, M. Vanbel, T. Verbiest, J. Rip, B. Brijs, T. Conard, C. Claypool, S. Takeuchi, S. Zaima, J. Mitard, B. D. Jaeger, J. Dekoster, and M. Caymax, Solid-State Electronics **60**, 116 (2011).
- ²⁷ R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, in 2011 Symposium on VLSI Technology Digest of Technical Papers (2011) pp. 56–57.
 ²⁸ K. Kite, S. Sumiki, H. Namma, T. Takakaki, T. Nickimur, and A. Tarimi,
- ²⁸ K. Kita, S. Suzuki, H. Nomura, T. Takahashi, T. Nishimura, and A. Toriumi, Japanese Journal of Applied Physics 47, 2349 (2008).
- ²⁹ D. Kuzum, A. J. Pethe, T. Krishnamohan, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, in 2007 IEEE International Electron Devices Meeting (Institute of Electrical and Electronics Engineers (IEEE), 2007).
- 30D. Monroe, Υ. Η. Xie, E. Α. Fitzgerald, Ρ. J. Silverman, and G. Ρ. Watson, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 11, 1731 (1993). 31
- ³¹ Q. Shi, M. A. Zudov, C. Morrison, and M. Myronov, Phys. Rev. B **91**, 241303 (2015).
- ³² O. A. Mironov, N. d'Ambrumenil, A. Dobbie, D. R. Leadley, A. V. Suslov, and E. Green, Phys. Rev. Lett. **116**, 176802 (2016).