Exploiting Dynamic Quantum Circuits in a Quantum Algorithm with Superconducting Qubits

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To date, quantum computation on real, physical devices has largely been limited to simple, time-ordered sequences of unitary operations followed by a final projective measurement. As hardware platforms for quantum computing continue to mature in size and capability, it is imperative to enable quantum circuits beyond their conventional construction. Here we break into the realm of dynamic quantum circuits on a superconducting-based quantum system. Dynamic quantum circuits not only involve the evolution of the quantum state throughout the computation but also periodic measurements of qubits mid-circuit and concurrent processing of the resulting classical information on timescales shorter than the execution times of the circuits. Using noisy quantum hardware, we explore one of the most fundamental quantum algorithms, quantum phase estimation, in its adaptive version, which exploits dynamic circuits, and compare the results to a non-adaptive implementation of the same algorithm. We demonstrate that the version of real-time quantum computing with dynamic circuits can yield results comparable to an approach involving classical asynchronous post-processing, thus opening the door to a new realm of available algorithms on real quantum systems.

The evolution of quantum information processing in real quantum systems has taken remarkable leaps in recent years, transcending from laboratory demonstrations to systems with reliability and performance suitable for cloud-based research access [1, 2]. Not long ago, experimental efforts largely focused on understanding the components that make up a quantum system, from understanding the limits to qubit coherence [3–5], state control [6–9], and readout [10, 11] with a significant amount of focus on developing improved two-qubit entangling gates [12–15] while lowering crosstalk [16–19]. Today there is a significant shift emerging towards implementing quantum circuits for exploring interesting new algorithms [20, 21] and as a tool for benchmarking the quality of a quantum computer [22].

A quantum circuit is a computational routine consisting of coherent quantum operations on quantum data, such as qubits, and concurrent real-time classical computation. Most early experiments with qubits involve quantum circuits that are simple in nature and consist of an ordered sequence of resets for qubit initialization, followed by quantum gates, and measurements. The simplicity of these circuits lies in the fact that they do not require any classical logic to be performed in the coherence time of the qubits. While this class is sufficient to implement the circuit model of quantum computing for practical implementations of quantum computing it is not enough for dynamic circuits that include quantum error correction, quantum teleportation, and iterative phase estimation, and even the measurement model of quantum computing [23, 24]. Dynamic circuits are circuits in which future states depend on outcomes of measurements that happen during the circuit.

Today, we are beginning to see emerging experiments where this classical *real-time* logic is built into the circuits. Examples include mid-circuit measurement [25, 26], mid-circuit reset [10, 27, 28], and demonstrations requiring low branching complexity such as quantum state and gate teleportation [29–32], state injection [33], and initial demonstrations of dynamic quantum error correction [34]. In these examples, the classical logic either requires no state information or only requires small amounts of information within simple algorithms. Therefore, these dynamic circuits can be implemented simply even for reasonably large systems. Here, we demonstrate a more demanding class of dynamic circuits with requirements for accurate quantum operations, measurements and resets as well as efficient handling of a large throughput of classical information in a time scale commensurate with the system's coherence. One of the protocols that better embodies the critical need for synergy between classical and quantum hardware in complex dynamic circuits is coincidentally an efficient version of the most important building piece of any quantum algorithm with a known exponential speed-up: the Quantum Phase Estimation (QPE) algorithm [35, 36]. With this demonstration we unveil a hitherto experimentally unexplored regime in quantum information processing. As quantum systems get increasingly accurate, longer lived, and faster queried, it is important to consider pathways for the processing of their classical outputs that does not limit the capability of the quantum system to compute, neither in time nor in breadth of resources. Our work signifies a first step towards dynamic circuits with non-trivial complexity.

QPE is a family of algorithms whose object is the efficient eigenvalue sampling of a Hamiltonian. Some flavors of QPE include the standard Quantum Fourier Transform (QFT) version [35, 36], approximate QFT methods [37], semiclassical QFT [25], Kitaev QPE [38], Iterative Phase Estimation (IPE) [39–41], Heisenberg-limited QPE [42], and Bayesian QPE [43, 44]. QPE has been studied theoretically in noisy systems before [46] and alternative methods have been proposed that accelerate the learning at the cost of -potentially exponential- classical post-processing of the outputs [47]. In this work, however, we want to assess the impact on the QPE algorithm of real-time classical operations on quantum systems and the exploitation of dynamic circuits.

QPE is concerned with the problem of estimating an eigenvalue ϕ given the corresponding eigenstate $|u\rangle$ for the unitary operator U, with $U|u\rangle = e^{i\phi}|u\rangle$.

We can use a quantum register to encode the eigenstate $|u\rangle$,

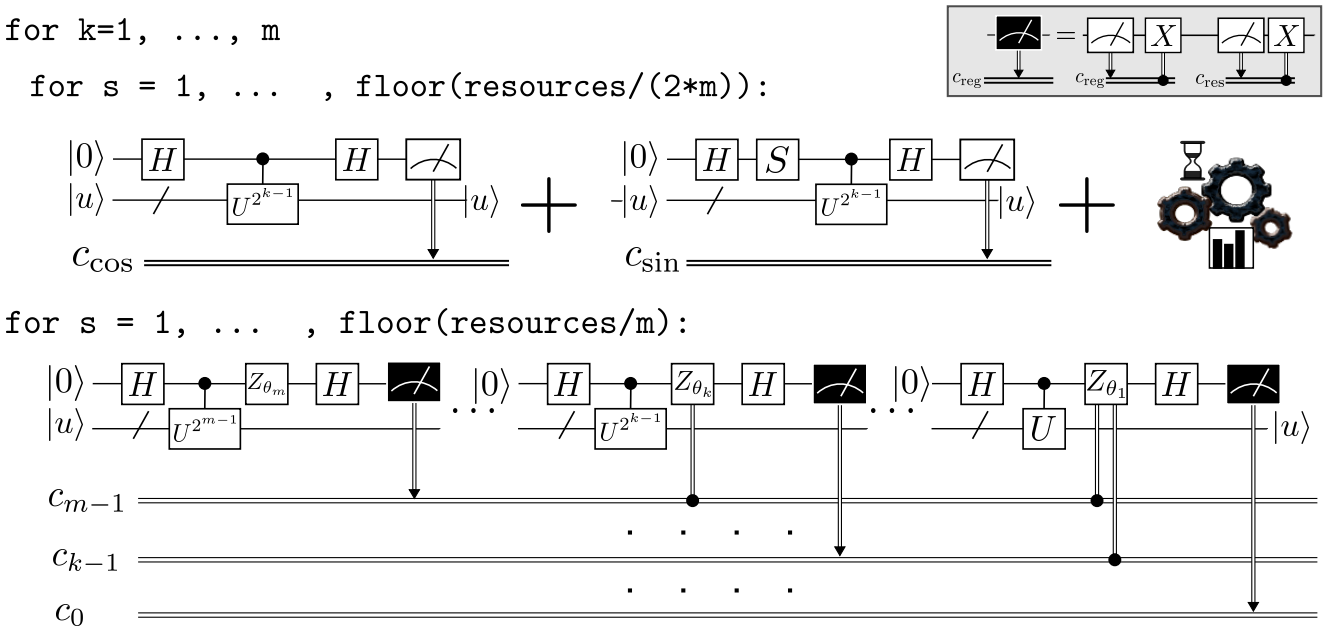

FIG. 1: Circuit diagrams for m-bit implementations of QPE using the two approaches described in this work: Kitaev's QPE (top) and IPE (bottom). The variable s guides the cumulative average of each circuit sampling up to its final amount determined by the total number of resources (measurements). Note that for the IPE case (top right gray box) a resource includes the conditional reset of the qubit, which is run twice. The Kitaev circuits do not need previous knowledge of other bits at the expense of running and measuring one extra circuit per bit and needing additional near-time computing resources [45]. The iterative version uses a $Z-$rotation conditional on all the previous measured bits before measuring the auxiliary qubit in the X-basis.

and an auxiliary system, which we can call the pointer, to extract the phase. The simplest method for solving this problem is to run the left-hand side circuit in the top panel of Fig. 1 with $k = 1$. By preparing the pointer qubit in the $|+\rangle$ state and using it as the control in a controlled-U operation, the phase ϕ can be transferred from the eigenstate register to the pointer. If we define $\varphi = \phi/2\pi$, sampling the distribution obtained when measuring the pointer in the $x-$basis will give us the $m-$bit approximation $\tilde{\varphi} = \sum_{k=1}^{m} \varphi_k/2^k = .\varphi_1\varphi_2\ldots\varphi_m$ with $\varphi_k \in \{0, 1\}$, with $|\tilde{\varphi} - \varphi| \leq 1/2^{m+1}$, where we use the standard dot notation for a binary expansion. This approach is exponentially costly in m [48].

Kitaev's original approach to QPE uses the two families of circuits depicted in Fig. 1 (top). From these circuits, we can obtain an approximation to the quantities $\alpha_k = 2^{k-1}\tilde{\varphi}$ which shift the bits in φ to the left by k positions [48]. The two types of circuits are needed to lift the sign uncertainty in α_k. These phase shifts can then be used within a classical iterative algorithm to reconstruct our approximation to the phase $\tilde{\varphi}$ with $m\log(m)$ overhead [48].

One could do better than this approach by exploiting dynamic circuits. By running the single dynamic quantum circuit in Fig. 1 (bottom), where measurements are interspersed throughout the circuit and classical information is processed within the duration of it, we can economize in the number of resources spent and eliminate the need for the classical post-processing. This is the IPE approach, where each of the measurements of the pointer following a controlled-$U^{2^{k-1}}$ provides the *kth*-bit φ_k directly. The IPE algorithm thus builds the phase from least to most significant bit, and is adaptive in nature, meaning that the exact configuration of the circuit gates depends on the outcomes observed in the measurements performed throughout the circuit itself, via the argument $\theta_k/2\pi = -.0\varphi_{k+1}\varphi_{k+2}\ldots\varphi_m$, where $\theta_m = 0$. In the absence of noise, it can be shown [49] that a single measurement of the pointer for each sub-circuit gives an $m-$bit approximation to the phase with probability higher than $8/\pi^2$.

For these experiments, we use two superconducting transmon qubits [50] in a 14-qubit quantum processor (see [48], including references [51–57]). Both the qubit to qubit coupling and the qubit readouts are mediated by coplanar waveguide resonators [58]. Qubit readout and conditional reset [10] are critical parts of this work (see [48] for more readout details, including references [59–68]), and the successful performance of a measurement and reset cycle relies not only on the dynamics of the qubit-resonator interaction, but on efficient classical electronics hardware and software [11, 69]. Here we use a field programmable gate array (FPGA) platform to measure and control our quantum system, as well as for feedback (here understood as conditional qubit reset following a measurement) and feed-forward (conditional operations as required by the algorithm) [33, 48].

The readout and conditional reset of our pointer qubit is a critical aspect of this work. Fig. 2 shows different aspects of our measurement and reset protocol. We prepare the qubit

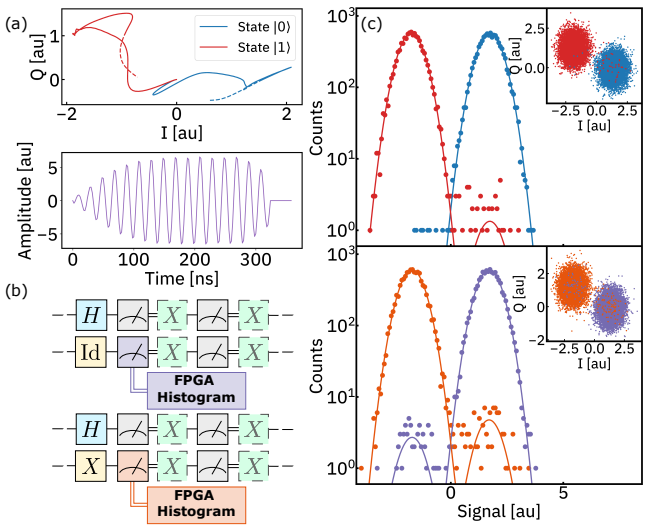

FIG. 2: Qubit measurement and reset of the pointer qubit. (a) I/Q traces (upper plot) and discriminator kernel (lower plot). The readout signal is sampled for 360 ns (dashed in I/Q traces) and the kernel is applied for 320 ns (solid in I/Q traces). (b) Experimental sequences to assess qubit reset quality. The sequences are played in order from top to bottom at a repetition rate of 100 kHz. After each computational state is prepared, the first measurement is used to build the histograms in the bottom panel of (c). The shaded X-gates are applied conditionally to the preceeding measurement outcome being 1. (c) Histograms from preparing each computational state 10,000 times at 1 kHz (top) and 100 kHz (bottom). From the histograms we extract an assignment error of 3×10^{-3} (top) and 8.3×10^{-3} (bottom). The insets show the integrated samples in the I/Q plane.

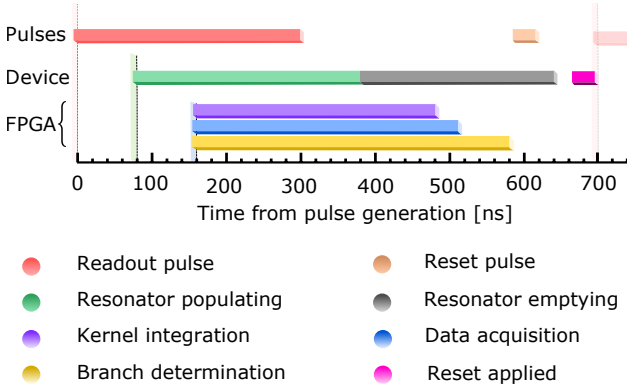

FIG. 3: Latency breakdown in a measurement and reset cycle. The control electronics entire latency to determine the qubit state, send a conditional marker to a blanking switch, and determine the IPE branching path, is comparable to the latency due to resonator dynamics (population and emptying). This cycle is repeated twice during the algorithm, yielding a total qubit reset latency of 1.4 μs.

in the states $|0\rangle$ and $|1\rangle$ and use its readout signal statistics to calibrate a kernel for qubit state discrimination [70, 71]. Fig. 2(a, top) shows the I/Q trajectories of the demodulated signals for $|0\rangle$ (blue) and $|1\rangle$ (red). Fig. 2(a, bottom) shows the discriminator kernel, which is computed as the difference between the average signals from the qubit $|0\rangle$ and $|1\rangle$ states. We characterize our readout fidelity by gathering statistics of the readout signal from the two qubit states and binning the integrated shots. The histograms for both states are shown in Fig. 2(c, top) for $|0\rangle$ (blue) and $|1\rangle$ (red). In order to minimize state preparation error, these shots are taken at 1 kHz repetition rate, which allows the qubit to thermally relax to its ground state in between experiments. We then look at the result of running the same experiments at 100 kHz repetition rate, which is faster than the qubit relaxation time. In this case, we precede each qubit state preparation by an initialization sequence consisting of a positive 90-degree rotation around the X-axis, followed by two conditional qubit resets. The four alternating sequences are shown in Fig. 2(b), with the corresponding histograms and integrated shots shown in Fig. 2(c, bottom). The reset error after two cycles of conditional reset is 0.01 [48].

The real-time computing part of the IPE algorithm has two main components: the application of a bit-flip gate to the pointer qubit conditioned on its measurement yielding the state $|1\rangle$ (qubit reset) and the determination of the $Z-$rotation angle θ_k for each subsequent circuit. The former determines the measurement and reset latency cycle, which we can define as the elapsed time between the measurement tone being fired at room temperature and the system (room temperature electronics plus quantum processor) being ready for a new operation (gate or measurement). Our experimental latencies for this cycle are shown in Fig. 3. There are two main independent timelines: the readout resonator dynamics and the control electronics latencies and delays. A cable length (plus internal electronics) latency of 160 ns adds an additional constant shift to the relative timings. We have separated the different contributions to the total cycle length vertically in Fig. 3 for clarity. Defining as $t = 0$ the instant the 300 ns long readout pulse is sent by the control electronics, we reach the state determination at 488 ns (purple bar). At this time, the FPGA logic operates the blanking switch that screens the reset tone (peach bar), which is applied at 585 ns and reaches the qubit some time later (pink bar). Meanwhile, at the quantum processor, the readout resonator empties of readout photons at a rate determined by the resonator $Q \sim 1150$ (gray bar). Even though the reset pulse is sent at a time when the resonator is still slightly populated, the additional cable and electronics internal latency justifies our placement of the qubit reset pulse at 585 ns. This offers a reasonable trade-off between avoiding both resonator residual population and qubit decay effects. Finally, a few tens of ns are added to the entire cycle due to constraints related to the ADC sampling rate and the need for consistency in the measurement phase for kernel discrimination. It is important that the determination of the conditioned phase rotation happens within the described measurement and reset cycle, so as to not add further delay in the algorithm when implementing this part of the real-time computing. In our experiments, the IPE algorithm is encoded in

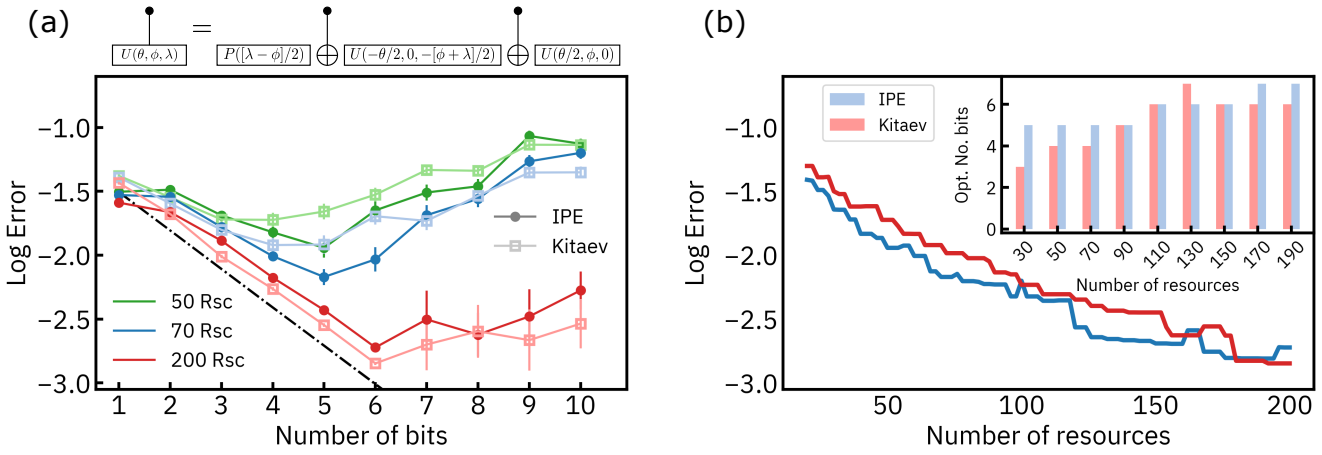

FIG. 4: (a) (Top) Decomposition of a controlled-U, where U is a parameterized element of $SU(2)$, in terms of single-qubit unitaries (U rotations and the phase gate P -see [48] for details on the P-gate) and CNOTs. (Bottom) Phase estimation error up to 10-bit accuracy for both algorithms when the total number of resources are kept constant at 50, 70, and 200. The lower bound of the error is shown for each bit as a dash-dotted black line. (b) Algorithm error as a function of the number of available resources for IPE (blue) and Kitaev (red). The lowest error is chosen among the available number of bits for a given number of resources for both algorithms. The optimal number of bits for a discrete set of resources for both protocols is shown in the inset.

software as a branching protocol [48], with the branch determination taking place after each of the IPE circuits shown in Fig. 1 (bottom). We can see in Fig. 3 that the branch determination latency (yellow bar) falls well within the measurement and reset cycle limits.

For our experiments, we encode these phases as eigenvalues of the Pauli operator X. With this choice of U we aim at maximizing the exposure to decoherent noise of the eigenstate-encoding qubit. Once an operator U for the problem has been chosen, we can implement a controlled-U operation using only CNOT and $SU(2)$ unitaries on the target as shown in Fig. 4(a, top). In order to extend our experimental reach and the comparison range for both protocols, we implement each controlled-$U^{2^{k-1}}$ not by repeated applications of controlled-U, but by a single application of a controlled-U' where $U'|u\rangle = e^{2^{k-1}i\phi}|u\rangle$. This is an important requirement, as efficient implementations of powers of U in the QPE algorithm are critical to obtain an exponential speed up. With this approach, each implementation of the controlled-$U^{2^{k-1}}$ in the circuits in Fig. 1 contains just two CNOTs.

We define a resource as the physical act of measuring a qubit. For a given number of available resources R and bits m, we sample the circuits in Fig. 1 $\lfloor R/2m \rfloor$ times in the Kitaev case and $\lfloor R/m \rfloor$ times in the IPE case, as Kitaev's protocol calls for 2 measurements per bit. We implement the IPE and Kitaev's protocols up to 10 bits and for 600 different phases chosen randomly from the interval $[-\pi, \pi)$. The results for both protocols at 50, 70, and 200 measurement resources are shown in Fig. 4 (a, bottom). We see, for a given number of resources, that both algorithms initially show an improvement in the phase estimation accuracy as the number of bits increases. The total resources available keep getting distributed equally among bits and thus above some bit number, the algorithm performance starts to suffer. In the case of the IPE algorithm, the circuits also become deeper with increased number of bits. We observe that, despite these deeper circuits and the latency associated with qubit measurement feedback and feedforward, the IPE approach provides comparable results to Kitaevs classical post-processing. When the number of bits is not restricted and only the number of resources is limited, we find that IPE gives lower errors on average below around 100 resources (Fig. 4 b). As the number of available resources is increased, both algorithms become comparable both in the error and in the optimal number of bits (Fig. 4 b, inset).

The experiments shown in this work demonstrate that quantum computing hardware has reached a level of maturity where it can benefit from dynamic circuits. In these circuits the performance of a quantum algorithm can depend on the the classical real-time computing architectures. This demonstration of QPE in a solid-state system can be considered as a first step towards larger scale demonstrations of algorithms that can exploit dynamic circuits and shows that a carefully designed quantum system must take into account all of the components (quantum processor, readout, control electronics, and software). As we build to larger more powerful systems we expect dynamic circuits to be the core for future quantum circuit libraries, algorithms and applications.

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