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Improved error thresholds for measurement-free error correction

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Motivated by limitations and capabilities of neutral atom qubits, we examine whether measurement-free error correction can produce practical error thresholds. We show that this can be achieved by extracting redundant syndrome information, giving our procedure extra fault tolerance and eliminating the need for ancilla verification. The procedure is particularly favorable when multi-qubit gates are available for the correction step. Simulations of the bit-flip, Bacon-Shor, and Steane codes indicate that coherent error correction can produce threshold error rates that are on the order of 10^{-3} to 10^{-4} —comparable with or better than measurement-based values, and much better than previous results for other coherent error correction schemes. This indicates that coherent error correction is worthy of serious consideration for achieving protected logical qubits.

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An important near-term goal in quantum information processing is the construction and operation of a high-quality logical qubit. This goal is currently being pursued in several physical systems [1–4]. One promising candidate system is an array of neutral atoms held in optical or magnetic traps [5, 6]. The quantum information is stored in atomic hyperfine clock states. This system has several attractive features: each natural qubit is identical, clock states exhibit long coherence times measured in seconds, and state preparation and state measurement can be performed on msec timescales using well-developed techniques of optical pumping and detection of resonance fluorescence [7, 8]. Arrays of individually addressable neutral atom qubits have been demonstrated in 1D [9, 10], 2D [11–14], and 3D [15]. Qubit numbers of order 100 have been demonstrated in 2D and 3D and in principle these numbers could be extended to several thousands using available technology. Lastly, the available gate set is universal, based on microwave and laser light for single qubit rotations together with Rydberg state mediated interactions for two-qubit, and multi-qubit, entangling gates [6].

Achieving logical protection requires an error correction procedure compatible with available operations. Standard error correction protocols rely on performing frequent syndrome measurements [16, 17]. This turns out not to be well suited for neutral atom implementations for two reasons. First, the time needed for state measurements is currently several orders of magnitude longer than for gate operations. Second, it is difficult to measure a single atomic qubit in an array without scattered light corrupting the state of nearby qubits, although a number of possible solutions to this problem are under study [18].

These challenges motivate the consideration of coherent, or measurement-free, error correction (CEC) methods [19–22]. Like standard measurement-based error correction (MEC) [1–4], techniques for measurement-free error

correction are based on stabilizer codes. However, there has been strong skepticism that CEC can produce error thresholds close to those of MEC [23–25], though Paz-Silva *et al.* did achieve a CEC threshold only about one order of magnitude worse than MEC [20]. We improve this result by nearly 2 orders of magnitude by taking advantage of the resources available to neutral atoms, in combination with a novel syndrome extraction technique.

CEC is particularly attractive for neutral atom and trapped ion approaches that rely on light scattering for entropy removal. As part of an error correction cycle, entropy in the data qubits is transferred to fresh ancilla qubits, and is subsequently removed by resetting the ancillas. Although an ancilla reset requires optical pumping and light scattering, the number of scattered photons is typically 1–2 orders of magnitude less than would be needed for state measurement in MEC.

CEC can additionally benefit from an additional resource of neutral atom systems, since the computational capabilities include native Toffoli and C_k NOT gates. These C_k NOTs can potentially achieve fidelities as high as 90% for $k \sim 35$, while for smaller k the fidelities of the native gates are expected to beat fidelities of the decompositions into 1- and 2-qubit gates [26, 27]. Similarly, Rydberg interactions allow for parallel CNOT gates in which a single control qubit targets multiple qubits simultaneously, improving the time required for syndrome extraction. Native Toffoli gates have also been demonstrated using trapped ion [28] and superconducting qubits [29], and these gates have been used for CEC with superconducting qubits [30]. Thus the techniques presented here could potentially be adapted to other platforms.

A quantum error correction code is determined by the number of physical qubits and by the stabilizing group that fixes the logical subspace. This stabilizer group, with elements S_i , is determined by its generators. Given n stabilizer generators, we can consider $2^n - 1$ distinct

TABLE I. Correctly extracted syndromes for single-qubit bit-flip errors on the logical $|000\rangle$ state. The table is easily extended to errors on the $|111\rangle$ state.

	$ 000\rangle$	$ 100\rangle$	$ 010\rangle$	$ 001\rangle$
Z_1Z_2	0	1	1	0
Z_2Z_3	0	0	1	1
Z_1Z_3	0	1	0	1

non-trivial products of the generators, forming additional stabilizers. If stabilizer values could be extracted and processed without error, only the stabilizer generators need to be measured, and additional stabilizers would not provide additional useful information. The procedure we propose is to copy onto ancillas the redundant information of a subset of these additional stabilizers. This enables one not only to identify data errors, but also errors that occur during syndrome extraction. The redundancy becomes useful when combined with the Toffoli and C_k NOT gates, where the quantum gates act as logical ‘AND’ gates to ensure that stabilizer values agree, conditionally targeting errors only if extracted stabilizer values match expected syndromes. Using this method, the ancilla qubits store only classical information—i.e., they are immune to phase errors and are not directly entangled with each other. We discuss this approach for three codes: 3-qubit bit-flip, 9-qubit Bacon-Shor, and 7-qubit Steane.

The 3-qubit bit-flip (BF) code has logical states $|0\rangle_L = |000\rangle$ and $|1\rangle_L = |111\rangle$ with the usual stabilizers

$$S_1 = Z_1Z_2; \quad S_2 = Z_2Z_3.$$

The values of S_1 and S_2 correctly identify single-qubit errors, and each syndrome value corresponds to a distinct correction procedure. Thus, any extraction errors leading to an incorrect value of either stabilizer leads to an incorrect procedure, likely resulting in a logical error. However, by considering the additional stabilizer

$$S_3 = S_1S_2 = Z_1Z_3$$

it is possible to correctly identify if a single error occurs during ancilla preparation or syndrome extraction (collectively: extraction errors). This property follows from the fact that a correctly extracted syndrome always produces an even number of ancillas in the logical $|1\rangle$ state, as shown in Table I. Therefore, a single extraction error occurs if an odd number of ancilla qubits occupy a logical $|1\rangle$ state. The error-correction circuit is shown in Fig. 1. The circuit makes use of C_3 NOT gates, to correct errors on the data qubits only if the ancillary state corresponds to a valid syndrome.

An advantage of using additional stabilizer information is that the procedure does not require separate an-

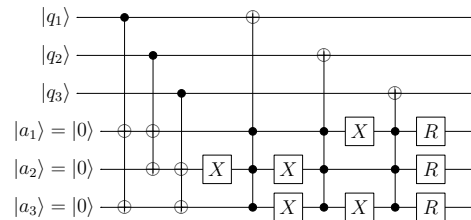


FIG. 1. The full measurement-free extraction and correction circuit for the BF code. The first 3 gates are for syndrome extraction. The combination of X gates and C_3 NOT gates detect properly extracted syndromes and correct errors accordingly. If a syndrome value is incorrectly extracted, the data qubits are not affected. Reset operations are performed in the final step, indicated with R operations. This circuit also demonstrates the bit-flip correction procedure for the BS code, taking each $|q_i\rangle$ to be a row in the BS code. Then each CNOT gate is interpreted as 3 CNOT gates, one controlled by each qubit in the row. The C_3 NOT gates target any single qubit in the row. A similar procedure is required for phase errors in the BS code.

cilla verification. That is, single-qubit extraction errors can be detected simply from the combinatorics of properly extracted syndromes. In our CEC circuits, the C_k NOT gates act nontrivially on data qubits—i.e. correct errors—only if syndromes are properly extracted. This implies that pre-existing data errors can survive a faulty CEC cycle. However, with high probability the surviving data error is simply corrected during the following cycle.

The 9-qubit Bacon-Shor (BS) code is obtained by layering the bit-flip code, with one layer designed to protect against phase errors, resulting in a code that can correct arbitrary single-qubit errors. The logical X and Z operators are just $X^{\otimes 9}$ and $Z^{\otimes 9}$, respectively. The error correction procedure is quite similar to the bit-flip code, still needing just 3 ancillas. Due to the underlying symmetry, this code requires only 4 stabilizer generators. With the data qubits in a 3×3 grid, the stabilizers are:

$$Z_U = \begin{pmatrix} Z & Z & Z \\ Z & Z & Z \\ I & I & I \end{pmatrix}, \quad Z_D = \begin{pmatrix} I & I & I \\ Z & Z & Z \\ Z & Z & Z \end{pmatrix},$$

$$X_L = \begin{pmatrix} X & X & I \\ X & X & I \\ X & X & I \end{pmatrix}, \quad X_R = \begin{pmatrix} I & X & X \\ I & X & X \\ I & X & X \end{pmatrix}.$$

The procedure to perform error correction then proceeds in a manner similar to the BF code. To correct bit-flip errors, we consider the additional stabilizer Z_UZ_D . The circuit then proceeds as in Fig. 1 but now taking each $|q_i\rangle$ to correspond to a single row of 3 data qubits. Each CNOT gate in the circuit can then be interpreted as 3 physical CNOT gates—one for each data qubit. The C_k NOT gates can target any single physical qubit in the row. The procedure for correcting phase errors is analogous, although extraction and correction is done by col-

umn. Additional information is provided in the supplementary material.

The 7-qubit Steane code has 6 stabilizer generators and requires 7 ancillas to correct arbitrary single-qubit errors. Three Z -type stabilizers

$$S_1^Z = Z_1 Z_2 Z_3 Z_7; \quad S_2^Z = Z_1 Z_2 Z_4 Z_6; \quad S_3^Z = Z_1 Z_3 Z_4 Z_5$$

detect bit-flip errors, while X -type stabilizers detect phase-flip errors and are obtained from the Z -type operators by replacing each Z_i with X_i . The logical operators are $Z_L = Z^{\otimes 7}$ and $X_L = X^{\otimes 7}$

We will restrict our discussion to bit-flip errors; phase errors follow analogously. With 3 Z -type generators, we can form 7 distinct stabilizers. Then error correction proceeds as follows: (1) extract the 7 stabilizer values onto 7 ancilla qubits, and (2) use a sequence of 7 C_4 NOT gates to correct errors, matching each target data qubit q_i to the unique set of control ancilla qubits whose corresponding stabilizers act on q_i . The details of this procedure are discussed in the supplementary material, and the circuit is shown in Fig. 2.

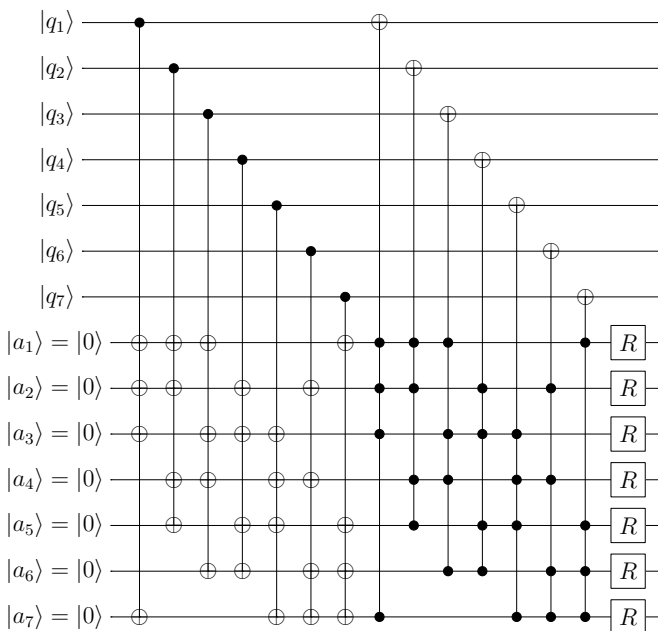


FIG. 2. Error correction circuit for the Steane code for bit-flip errors. The circuit for phase errors is similar.

We performed a numerical simulation of measurement-free error correction using the circuits shown in the previous section. We adopted an error model controlled by two error-rate parameters: the gate rate p_{gate} , and the memory (or idle-gate) rate p_{mem} . All single-qubit gate errors are all assumed to be depolarizing, i.e. if an error occurs on qubit i , then a single-qubit Pauli is selected at random and applied to qubit i . Two-qubit gate errors occur with the same probability p_{gate} as single-qubit

TABLE II. Comparison of CEC and MEC gate thresholds. The BS and Steane MEC values are the best values obtained for each code in Ref. [34], while the BF value is obtained from [35] and is scaled by 1.5 since our error rate includes phase errors.

	BF	BS	Steane
CEC $p_{\text{mem}} = 0$	0.010	1.8×10^{-3}	8.9×10^{-5}
CEC $p_{\text{mem}} = p_{\text{gate}}$	5.5×10^{-4}	1.01×10^{-4}	3.2×10^{-5}
MEC $p_{\text{mem}} = 0$		2.6×10^{-4}	5×10^{-4}
MEC $p_{\text{mem}} = p_{\text{gate}}$	~ 0.03	2.1×10^{-4}	2.6×10^{-4}

gates, but the error is chosen at random from the set of 2-qubit Paulis. For multi-qubit gates, each control-target pair of qubits is treated as a two-qubit gate site, subject to error model as other two qubit errors. The effect is that C_k NOT gates have an error rate of roughly $k \cdot p_{\text{gate}}$, roughly matching physical error models [27]. This model is discussed further in the supplementary material.

The simulated circuits required the ability to perform single-qubit Pauli, CNOT, and C_k NOT gates. The state evolution was performed using stabilizer simulation, in a manner similar to the techniques outlined by Aaronson and Gottesman in [31]. However, the C_k NOT gate is not in the Clifford group, and is not typically simulable in an efficient manner. However, in every circuit studied here, the C_k NOT gates are always controlled by the ancilla qubits, which only store classical information and are modeled as classical bits.

To efficiently collect data on the circuit, we used simulation and computational techniques similar to those in Refs. [32] and [33], with additional detail in the supplementary material. Using these techniques, we can easily and accurately estimate logical error rates. In principle, these methods could be scaled to more qubits and additional input parameters in a straightforward manner.

The threshold was evaluated by determining p_{gate} such that the logical error rate p_{log} satisfied $p_{\text{log}}(p_{\text{gate}}) = p_{\text{gate}}$. To reduce p_{log} to a function of a single parameter, we set p_{mem} to a fixed value, or set $p_{\text{mem}} = p_{\text{gate}}$. For neutral atom qubits, memory error rates are one to two orders of magnitude below gate rates. In this region of parameter space, varying p_{mem} had little effect on the threshold gate rate, demonstrated in Figs. 3 and 4. The threshold results are summarized in Table II.

The difference between the thresholds for the Bacon-Shor and Steane codes highlights the behavior of C_k NOT gates with unprotected ancilla qubits. In the Steane code, the successful correction of a data error depends on the successful extraction of 4 syndrome values, while the Bacon-Shor depends on only 3 syndrome values. Furthermore, the syndrome extraction process for the Steane code requires 56 CNOT gates, compared with 36 for the

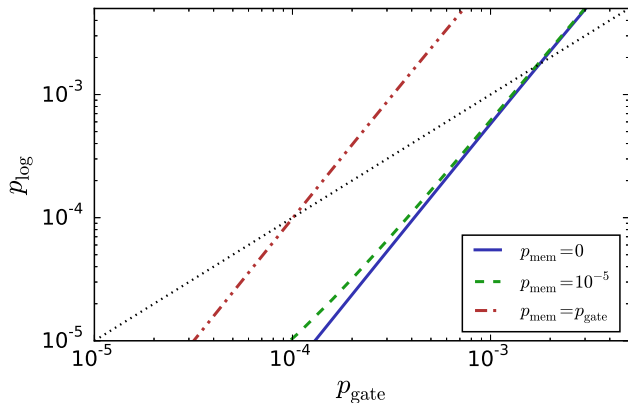


FIG. 3. (Color online) Logical error rate vs. gate error rate for the Bacon-Shor code, with three different choices of memory error rate. The dotted line shows $p_{\text{log}} = p_{\text{gate}}$. The difference between the curves with memory rates of 0 and 10^{-5} is minimal.

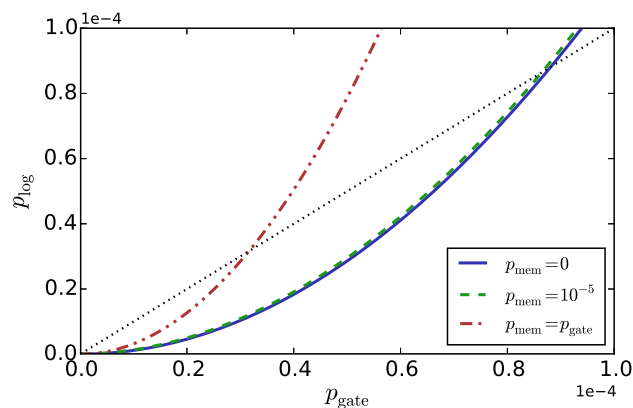


FIG. 4. (Color online) Logical error rate vs. gate error rate for the Steane code, with three different choices of memory error rate. The dotted line shows $p_{\text{log}} = p_{\text{gate}}$. Note the near overlap between the curves with memory rates of 0 and 10^{-5} .

Bacon-Shor code. Thus, the C_k NOT gates performing error correction are significantly more likely to fail in the case of the Steane code. However, in all procedures studied here, failures in extraction do not propagate *new* errors onto data qubits.

Earlier work on measurement free error correction found a threshold of $p_T \approx 3.8 \times 10^{-5}$ for the 9-qubit Bacon-Shor code [20]. Thus, our work indicates a substantial improvement over this value. Additionally, the earlier value needs 18 additional ancilla qubits, while our protocol needs just 3. The differences can be attributed to the combination of extracting additional stabilizer values, coupled with the efficiency of C_k NOT gates for performing classical logic.

Directly comparing our result to measurement-based results is not straightforward – measurement-based val-

ues depend on the chosen ancilla verification scheme and do not use extra stabilizer information. In addition, there is some arbitrariness in our choice of an error model for C_k NOT gates. With these caveats, in Table II, we compare our results to the best measurement-based threshold values from Ref. [34], which are also first-level depolarizing thresholds. The dramatic difference in thresholds for the case of the Bacon-Shor seems to exist only in the regime where memory error rates are small. In this regime, errors are dominated by gate errors, but the circuit lengths for CEC using neutral atom resources are typically quite small – and certainly smaller than those required for ancilla verification. Without the efficiency of multiqubit resources, we would expect thresholds to drop.

Somewhat surprisingly, the thresholds calculated for CEC are comparable to, and, in the case of Bacon-Shor, better than thresholds calculated for MEC. The threshold error rates for the bit flip and Bacon-Shor codes are above 10^{-4} (10^{-3}) with (without) memory errors. It has been shown theoretically that Rydberg gates with shaped pulses can achieve a gate error below 10^{-4} [36]. Furthermore the scaling of the C_k NOT error with k is sublinear for small k growing to quadratic for k above about 15 [26, 27]. We infer that implementation of CEC with Rydberg gates while challenging, is theoretically possible. The overhead required for CEC is not greater, and possibly even less than that in MEC, though C_k NOT gates are required. Furthermore, the technique of using redundant syndrome extraction can potentially be useful in other architectures. Certainly, measurement problems are not restricted to neutral atoms. Furthermore, redundant syndrome extraction can potentially be used in MEC to avoid ancilla verification, which we plan to explore in future research.

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