Microscopic Origin of the Reduced Thermal Conductivity of Silicon Nanowires

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Phys. Rev. Lett. **108**, 215901 — Published 21 May 2012

DOI: 10.1103/PhysRevLett.108.215901

Microscopic origin of the reduced thermal conductivity of silicon nanowires

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(Dated: April 6, 2012)

We designed nanowires with tailored surface structure and composition and with specific core defects, to investigate the microscopic origin of the reduced thermal conductivity of Si at the nanoscale. We considered a diameter (15 nm) comparable to that of systems fabricated in recent experiments and we computed the thermal conductivity using equilibrium molecular dynamics simulations. We found that the presence of a native oxide surface layer may account for a 10 to ∼30 fold decrease in conductivity, with respect to bulk Si, depending on the level of roughness. However it is only the combination of core defects and surface ripples that enables a decrease close to two orders of magnitudes, similar to that reported experimentally.

PACS numbers: 65.80.-g, 63.22.Gh

The search for Earth abundant and cheap materials for the conversion of thermal energy into electricity is an active field of research [1]. Promising candidates should be small band gap semiconductors with high mobilities, and much lower thermal conductivity than that of, e.g. bulk elemental semiconductors Si and Ge. A promising approach to lower the thermal conductivity (κ) of semiconductors, without significantly deteriorating their electronic properties is based on the growth of stable nanostructures and the design of nanocomposites.

In the case of Si, it has been shown that κ of nanowires (NWs) [2–6] (as well as that of the nano-porous material [7, 8]) may be substantially reduced with respect to that of the bulk, leading to a figure of merit (ZT) close to 1, that is almost two orders of magnitude larger than ZT of c-Si [9] (ZT is defined as: $\sigma S^2 T/\kappa$, where σ, S , κ and T are the electrical conductivity, the Seebeck coefficient, the thermal conductivity and the temperature, respectively). Although ZT $\simeq$ 1 is still far from the desired efficiency of solid state thermoelectric devices (ZT $\simeq$ 3 to 4) [1], it is a remarkable result to achieve such an efficiency for Si, which is a poor thermoelectric in its bulk form. However the origin of the increased figure of merit, and in particular of the much decreased thermal conductivity of Si at the nanoscale is still controversial.

The results reported by Li et al. [2] for VLS (Vapour-Liquid-Solid) grown Si NWs clearly showed that size reduction plays an important role in leading to the measured decrease in κ. Subsequent results by Hochbaum et al. [3] indicated that surface structure, roughness in particular, may also be a significant factor in determining the value of κ: indeed in Ref. [3] results for electroless etched (EE) wires with the same diameter as those studied in Ref. [2] were presented, showing much lower values of κ. Differences were also reported between the conductivities of EE wires obtained under different preparation conditions [5].

Several models and simulations [10–18] have appeared in the literature to provide a rationalization of experiments. There is general consensus that the surface structure may influence the conductivity of wires; in particular faceting of surfaces [18] has been recently investigated in detail, and shown to be responsible for great variations in κ, with an interesting interplay between facets and wires' growth direction. Roughness has been identified as playing an important role by several models, although there is disagreement on whether surface roughness alone may explain recent experiments, in particular the two orders of magnitude decrease in κ of wires, reported in Ref. [3].

Here we report atomistic simulations of heat transport in nanowires with a diameter (15 nm) comparable to that attained experimentally, and we provide, for the first time, realistic models of their structure, inclusive of ripples and silica oxide layers at the surface, and of core defects. We studied the interplay between surface composition, roughness and core defects, and we present a detailed microscopic analysis of the origin of the reduced conductivity, without resorting to models or assumptions on carriers' mean free paths. The effect of surface structure, composition and of core defects is studied by designing samples with tailored morphologies, in which structural parameters are varied one at a time.

We carried out a series of equilibrium molecular dynamics simulations (MD) for wires with diameter of 15 nm. Interatomic forces were described using parameterized Tersoff empirical potentials [19, 20], and simulations were carried out with the LAMMPS code [21]. We used cells of 10nm length in the direction of the heat propagation (z direction), amounting to about 95,000 atoms for each sample. Periodic boundary conditions were applied in the z direction, thus mimicking the simulation of an infinitely long nanowire. The thermal conductivity was obtained using the Green-Kubo formula:

$$\kappa_z = \frac{1}{k_B V T^2} \int_0^\infty < J_z(t) J_z(0) > dt, \qquad (1)$$

where k_B is the Boltzmann constant, V is the volume

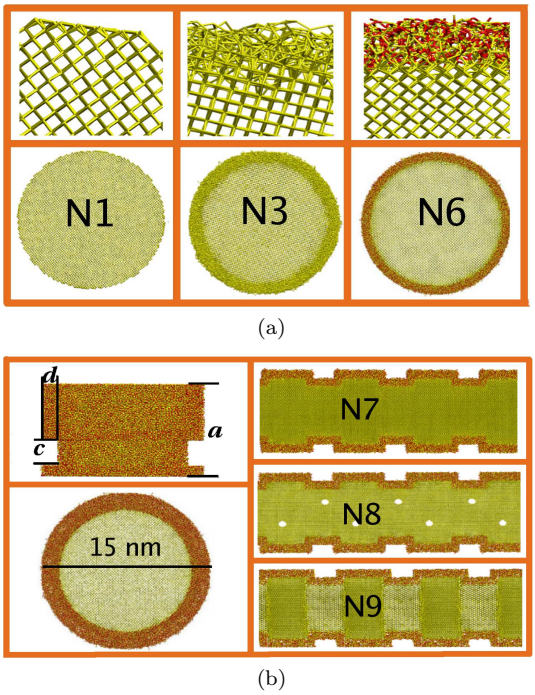

FIG. 1: Representative silicon nanowires generated in MD simulations. (a) Different surface terminations investigated in this study: reconstructed (sample N1), composed of an amorphous Si layer (sample N3) and of an amorphous silica layer (sample N6). (b)Samples with rippled surfaces (N7-N9) and with core defects (1 nm voids in N8 and grain boundaries in N9). The left hand side shows two cross sections of the wires grown along the z direction: upper part, (x,z) plane and lower part (x,y)plane. The a represents the length of the unit cell in our MD simulations; c is the distance between two ridges; and d is the depth of the valleys of rippled surfaces. For samples N7, N8 and N9 : a=10nm, c=3nm and d=1.5nm. All samples are described in detail in the text.

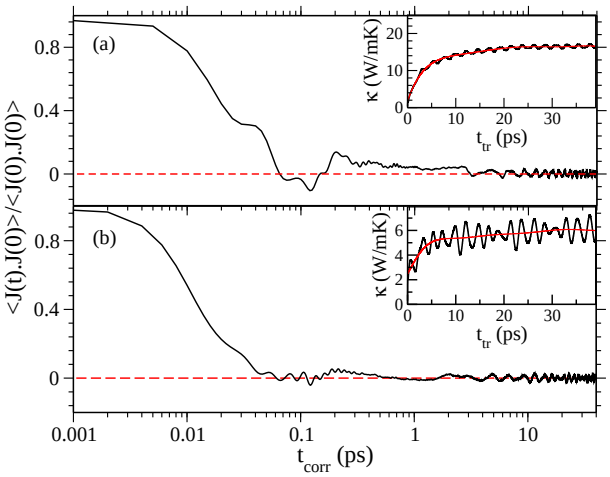

FIG. 2: The normalized heat current autocorrelation function of samples N3 (a) and N7 (b) shown in Fig. 1, as a function of the correlation time (t_{corr}) at room temperature. The insets show the calculated thermal conductivity as a function of the truncation time (t_{tr}) used in the evaluation of the integral in Eq.1.

of the system, and $< J_z(t)J_z(0) >$ is the average heat current ($\mathbf{J}$) autocorrelation function along the direction (z) of heat propagation.

The heat current is given by:

$$\mathbf{J} = \sum_{i}^{N} \epsilon_i \mathbf{v}_i + \frac{1}{2} \sum_{i,j;i\neq j}^{N} (\mathbf{F}_{ij} \cdot \mathbf{v}_i)\mathbf{r}_{ij}$$
$$+\frac{1}{6} \sum_{i,j,k;i\neq j\neq k}^{N} (\mathbf{F}_{ijk} \cdot \mathbf{v}_i)(\mathbf{r}_{ij} + \mathbf{r}_{ik}), \qquad (2)$$

where ϵ_i and $\mathbf{v}_i$ are the energy density and velocity associated to atom i, respectively. Vectors $\mathbf{r}$ denote interatomic distances between two atoms, and $\mathbf{F}$ interatomic forces.

In order to separate the effects of surface structure, roughness and core defects on the thermal conductivity of nanowires, we generated eleven different samples, all with the same diameter [22] and growth orientation (100), except for wires with grain boundaries, where we alternated (100) and (110) orientations. We first considered a wire (N1) with surfaces that were allowed to reconstruct (but not amorphize) during a 500 ps MD run at room T. Next we roughened the surface by adding an amorphous layer: the surfaces of nanowire 2 (N2) and 3 (N3) are composed of an amorphous silicon (a-Si) layer, generated by a heat and melt procedure, followed by an annealing cycle. To generate the atomic positions of N2 and N3, we carried out two separate simulations, where we heated sample N1 to 2400K and to 2800K for 500 ps, respectively [23], and we then decreased T to room temperature with a cooling rate of $10^{12} K/s$. By controlling the annealing T, we obtained amorphous layers of different thicknesses: 0.5 nm for N2 and 1 nm for N3. We then considered samples with rippled surfaces: the surfaces of samples 4 (N4) and 5 (N5) have ripples of the same width along the growth direction (see Fig.1b), but of different depths (d): d=0.5 nm and d=1.5 nm, respectively. Both samples have a thin (0.5 nm) a-Si layer at the surface.

Experimentally Si NWs are likely to be oxidized. Therefore we also considered samples with silica at the surface, as shown in Fig. 1a. First, we generated a bulk amorphous silica sample of dimensions 17.5nm X 17.5nm X 13.8nm by melting a SiO_2 crystal with the α-cristobalite structure, and then quenching the melt to room T. A structural analysis of the amorphous structure obtained in this way revealed a good agreement with experiment for partial correlation functions, structure factors and angular distribution functions [24]. We then embedded an ideally terminated 15 nm Si NW into the silica matrix, by removing a portion of the amorphous material. We froze the atoms in the core of the wire, i.e.

those occupying crystalline sites within approximately a 13 nm diameter; the atoms belonging to a thin Si surface layer and to the surrounding silica matrix were instead allowed to move; we heated up the sample to 6000K and then cooled it down to room T, with an annealing cycle of about 30ns and a cooling rate of $10^{12}K/s$. Finally, we removed the wire from the silica matrix with the desired thickness and shape of oxide at the surface (See Fig. 1b). Before collecting data for the calculation of the thermal conductivity, all wires terminated with silica were subjected to an additional annealing cycle of 5 ns, so as to remove as many interfacial point defects as possible. The surface of nanowire 6 (N6) is composed of a 1nm amorphous silica layer, whose thickness is directly comparable with that of the a-Si layer on N3. Nanowire 7 (N7) has rippled silica surfaces (as in the case of a-Si surfaces) with ripples that are 1.5nm deep. Finally, we considered samples (N8, N9, N10 and N11) with defects in the core. We generated N8 by introducing voids of 1 nm diameter in N7 with the concentration of 0.001 nm^{-3}. In a similar fashion, we obtained N9 from N7 by introducing grain boundaries, with contiguous (100) and (110) growth orientations. N10 has instead both vacancies and grain boundaries in the core. Finally N11 was obtained from N1 by introducing the same core defects as those present in N9, thus generating a wire with no surface disorder and only core defects. For each sample, the thermal conductivity was obtained as an average over 5 independent runs, with simulation times varying from 4 to 10 ns, depending on the degree of order in the sample. As an example of our computational procedure, and of the convergence of our MD simulations, we show in Fig.2 the heat current autocorrelation function as a function of simulation time, and the computed thermal conductivity as a function of the truncation time used to evaluate the integral of Eq. 1, for two representative samples.

Our results for the thermal conductivity of wires with 15nm diameters are shown in Fig.3. The thermal conductivity of the sample with reconstructed surfaces is reduced only by a factor of 3 with respect to that of bulk silicon (κ_{bulk}) [25], mainly because of boundary scattering, leading to a reduction of group velocities and lifetimes of the propagating heat carriers. To model the mere effect of mean free path reduction, we also computed the thermal conductivity of N1 using the Boltzmann transport equation (BTE) in the single mode relaxation time approximation. In particular, in the expression $\kappa = \sum_i c_i \tau_i v_i^2$, group velocities ($v$) and lifetimes ($\tau$) were calculated for bulk Si using anharmonic lattice dynamics, and the sum over i in the x and y directions was restricted to 15nm, i.e. the diameter of the wire.(c_i is the specific heat of mode i). We obtained a value of $\kappa_{bulk}/\kappa_{wire}$ (2.7) similar to that computed with MD (3). The value computed for κ of N1 is likely an upper bound to the thermal conductivity of non defective Si NW of 15 nm diameter: experimentally one expects a certain amount of disorder at the surface to

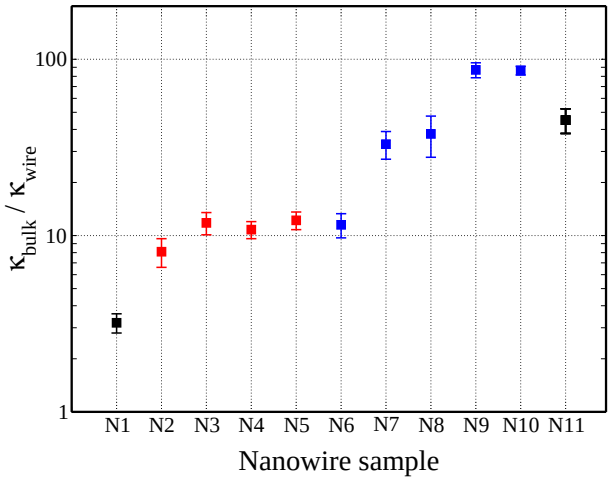

FIG. 3: Ratio between the computed thermal conductivity of bulk, crystalline Si (κ_{bulk}) and eleven Si nanowire (κ_{wire}) samples of 15 nm diameter, with different surface structure and composition, and with core defects (in the case of N8, N9, N10 and N11). Black squares: samples without amorphous surfaces; Red: samples with amorphous silicon surfaces; Blue: samples with amorphous silica surfaces. All samples are described in detail in the text (See also Fig.1.).

be present for any preparation condition, and disorder at the surface always leads to a decrease in κ. For example, adding an a-Si surface layer to N1 decreases its conductivity by a factor of 3 to 4, for N2 and N3, respectively; as expected, the thicker the amorphous layer, the lower κ. Based on our simulations of heat transport in a-Si and a-Si thin films [26], we expect that the conductivity of a completely amorphized wire will be of the order of 2W/mK and thus only in that case about 2 orders of magnitude smaller than that of bulk Si [27]. The decrease of conductivity in the presence of an amorphous layer partly originates from the presence of quasi-stationary modes, analogous to those found in a-Si [26, 28–30], that is of modes with mean-free paths of the order of inter-atomic distances; these modes carry heat, although much less efficiently than propagating modes. Interestingly, the composition of the surface layer appears to have little effect on the value of the computed conductivity, as shown by comparing the results obtained for N3 and N6, terminated by layers of a-Si and a-SiO_2 of the same thickness. In the presence of ripples, composition appears instead to have a non negligible effect, although we note that the shape of ripples turned out to be slightly different in a-SiO_2 and a-Si, which has smoother surface ripples.

Surface ripples lead to a sizable decrease of κ of crystalline wires with an amorphous surface layer. For example, the conductivity of samples N4 and N5, with ripples at the surface and the same thickness a-Si layer as sample N2, is about 1.5 times smaller than that of N2. When ripples were created on the surface of a wire (N7, see Fig. 1) with a-SiO_2 of 1 nm, the thermal conductivity dropped

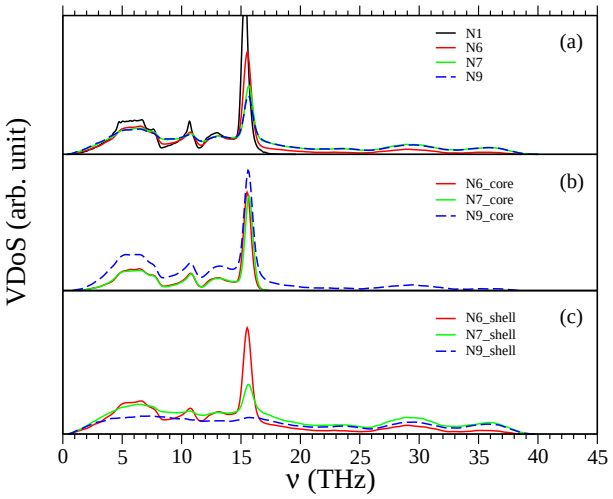

FIG. 4: Comparison of the vibrational density of states (VDoS) of samples N1, N6, N7 and N9 (See Fig.1), computed from the autocorrelation function of the atomic velocities. (a) full VDoS; (b) contributions to VDoS of the velocities of core atoms; (c) contributions to VDoS of the surface shells

by a factor of 3, leading to a 10-fold decrease with respect to N1 (no disorder at the surface) and more than a 30-fold decrease with respect to bulk Si. Fig.4 shows a comparison of the VDoS of samples N1, N6 ,N7 and N9, and we have separated the core (b) and surface components (c), in the case of N6, N7 and N9. These results show that the VDoS of wires with disordered surfaces are different from that of N1, over the entire frequency range. Likewise, the VDoS of the surface layer (or shell) of wires with rippled surfaces is substantially different from that of wires without ripples, again over the whole frequency range. We expect similar global changes to occur for the mode lifetimes. These results indicate that the presence of disorder at surfaces affect phonon-phonon scattering at all frequencies and thus plays an important role in decreasing the thermal conductivity of nanowires. Nevertheless disorder at the surface does not suffice to lower the conductivity by two order of magnitude, contrary to the case of thin rods[12]. It was only by introducing grain boundaries in the core of N7, that κ showed a reduction close to 100-fold. Interestingly Fig.4 shows that in the case of N9 not only the core component of VDoS differs from that of N7, but also the surface one, indicating again a global change in phonons. We note that the presence of 1nm voids in wires with rippled surfaces had a much weaker effect on the conductivity than the presence of grain boundaries. When the latter were present, the further addition of voids in the core did not substantially affect the conductivity. Grain boundaries have a large effect also on the conductivity of wires with no disorder at the surface, as can be seen from the value computed for N11, which is 14 times smaller than that of N1.

We now turn to the comparison with experimental results. Our wires with an amorphous surface layer (e.g. N6) are likely to resemble those obtained by VLS in Ref. [2]. The decrease in κ computed in our work (10-fold for a 15 nm wire) is smaller than that reported experimentally, with a conductivity of $\sim$ 8W/mK measured for a 22 nm wire (about 18-fold decrease). However we note that contact resistance may not be negligible in the experiments of Ref. [2], especially in the case of the thinnest nanowire. The experiments of Ref. [3] had instead wires with rough surfaces and, given the decrease reported for κ, we expect that the sample contained not only rippled surfaces but also a substantial amount of defects in the core; such defects may also be partially responsible for the moderate degrade observed in the electronic properties of the wires, compared to bulk Si. Furthermore, core defects may account for the differences between the results reported in Ref. [3] and Ref. [5] —where wires with rough surfaces and similar diameter as those of Ref. [3] were shown to exhibit larger values of κ. The comparison with the experiments of Ref. [4] is not straightforward, as the wires conductivity was estimated from that of an ensemble of functionalized wires. In general, an issue that remains to be addressed is the effect of contact resistance on the different measurements presented in the literature. In this respect the techniques pioneered in D. Cahill's group [31, 32] appear to be particularly promising.

Overall our results are in qualitative agreement with the model reported by Mingo et al. [33], showing that surface ripples may not be solely responsible for 2 order of magnitude decrease of the conductivity, contrary to the suggestions of Ref. [34]. Our analysis may be used to tailor the properties of silicon based materials for thermoelectric applications. In particular our findings indicate that fabrication requirements to obtain Si nanowires with the desired thermal conductivity, without degrading their electronic properties, are substantial, as surfaces and core defects need to be controlled with great precision.The use of polycrystalline Si with small grain sizes may represent a promising strategy. The optimal grain size will have to be optimized taking into account two conflicting requirements: the smaller the better to reduce kappa, however the smaller the larger the number of electronic trapping state density, which would decrease the electrical conductivity. Based on our previous results for np-SiGe [28], we expect that SiGe nanowires may be subject to less stringent constrains and work is in progress to investigate heat transport in SiGe thick wires, carrying out atomistic simulations.

We thank Davide Donadio,Ivana Savic, Deyu Li and Li Shi for useful discussions. Calculations were performed at the University of California Shared Computer Center on Mako cluster. Work supported by DOE/SciDAC-e under grant DE-FC0206ER25777.

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[24] A detailed analysis of our results for a-SiO_2 will be reported elsewhere.
[25] Here we considered the value of the thermal conductivity of bulk Si computed in a cubic cell of linear dimensions 10nm. The value is 198.39$\pm$20.86 W/mK. The value obtained with larger cells (e.g. with dimension 27 nm, containing 1,000,000 atoms) is 196.80 $\pm$ 33.28 W/mK.
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