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Memory States in Small Arrays of Josephson Junctions

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Abstract: We studied memory states of a circuit consisting of a small inductively coupled Josephson junction array and introduced basic (Write, Read, Reset) memory operations logics of the circuit. The presented memory operation paradigm is fundamentally different from conventional single quantum flux operation logics. We calculated stability diagrams of the zero-voltage states and outlined memory states of the circuit. We have also calculated memory access times and power dissipation for basic memory operations.

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Introduction

As conventional computing systems grow to very large systems (such as exascale computers) it is becoming increasingly important to reduce power consumption, reduce size, and increase the speed of a single computing operation. Such desire to study how to improve computing schemes led to some very interesting ideas of processor design based on quantum computing [1], biological computing [2], and nonlinear dynamics based chaotic computing [3].

One of the main challenges in modern computing systems is developing fast, small size, and energy efficient memory. As the requirements for memory grow immensely in modern times, so does the total cost to operate memory in exascale and other types of computing. One possible way to speed up memory access while reducing power consumption is cryogenic computing [4]. Cryogenic electronics based on superconducting devices (such as Josephson junctions, SQUIDS, etc.) that are generically very fast and energy efficient [5]. A single Josephson junction can operate at a speed close to THz, and switching between the states may require as little as $10^{-18} – 10^{-19}$ J (0.1 – 1 aJ).

Cryogenic memory plays an important role in development of superconducting-based computing. A variety of designs has been proposed including memories based on single flux quantum digital logic [6], hybrid superconducting-CMOS designs [7, 8], magnetic random access memory (RAMs) [9], and others [10]. Some of the main challenges in developing superconducting memory are reducing power dissipation, increasing access speed and reducing the size of the chip [10].

Superconducting single flux quantum digital logic circuits show promise to significantly advance performance in a variety of applications including computer CPUs, memories, digital radio frequency receivers and others [4]. The energy-efficiency of SFQ circuitry has significantly increased in recent years [10, 11]. However, designing RAMs still poses significant challenges and the slow development of

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cryogenic memory is one of the major bottlenecks for advancement in cryogenic supercomputing. While SFQ technology provides seemingly satisfactory solutions for cryogenic processing, only 4096 bits of memory have been demonstrated so far [6]. Moreover, when projected to a 1 PB memory, the power dissipation nears 85 MW, which is unacceptable [10].

In this paper we introduce a very simple memory paradigm based on the existence of multiple stable states present in a large variety of nonlinear systems. This paradigm is fundamentally different from a conventional paradigm that employs single flux quanta (SFQ) for memory operation. While we specifically address cryogenic memory based on small coupled arrays of Josephson junctions, the proposed paradigm may be more generic and applicable to systems other than cryogenic memory. Since we use junctions coupled through inductors, the stored energy in the circuit array can no longer be perfectly quantized. The equations of motion describing the dynamics of Josephson junctions in the framework of the resistively shunted junction (RSJ) model resemble the equations for physical pendulums with sinusoidal nonlinearity terms. Consequently, there are many systems that possess a similar type of nonlinearity [12]. In the proposed paradigm Read, Write, and Reset operations can be executed on the same circuit. Such systems may be highly tolerant to noise and disorder. In the absence of memory operations, the average voltage of each junction is zero, thus energy will dissipate only at the time of memory access operations. Both memory access times and energies can be minimal if the parameter set is chosen properly. The number of junctions and coupling design may vary, however it is desirable to operate a small array (2-3 junctions) to reduce the size of the system.

As an example, we present the principles of operation of a circuit consisting of three inductively coupled Josephson junctions by implementing a mathematical model. In our design, an inductively coupled array of three Josephson junctions operates at cryogenic temperatures (near 4 K) and is compact, fast, and energy-efficient. Write, Read, and Reset operations are applied to the same circuit to conserve area and decrease latency. Pulse energies required for implementation of the memory operations may be very low (in the range of 10^{-19} J (0.1aJ)) and delay times, measured from the application of the pulse to the circuit response, may be lower than 100 ps.

Memory Circuit Design

Our proposed memory circuit incorporates an inductively coupled array of three Josephson junctions with free-end boundary conditions. Figure 1 shows a schematic design of the proposed circuit.

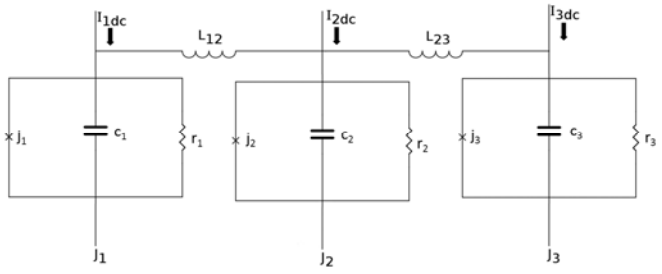

Figure 1: Schematic circuit diagram of three coupled RSJ Josephson junctions.

The following relations in Equation (1) define the current $I_{c,k}$ and the voltage V_k. The equation modeling an uncoupled resistively shunted junction (RSJ) circuit is provided by the Equation (2), below. This assumes operation in a cryogenic environment.

$$I_J = I_c \sin\phi, \quad V = \frac{\hbar}{2e}\frac{d\phi}{dt} \tag{1}$$

$$C\frac{dV}{dt}+\frac{1}{R}V+I_J=I_{ext} \tag{2}$$

Here I_j is the Josephson (superconducting) current on the junction, V is the voltage on the junction, C is junction capacitance, R is junction resistivity, I_c is junction critical current, I_{ext} is the external driving current, e is electric charge, and $\hbar$ is Planck's constant. Phase difference between the two parts of superconductors forming the junction is denoted by □. By combining Equations (1) and (2) we obtain the equation for the phase ϕ:

$$\frac{\hbar C}{2e}\frac{d^2\phi}{dt^2}+\frac{\hbar}{2eR}\frac{d\phi}{dt}+I_c\sin\phi=I_{ext} \tag{3}$$

The dimensionless equation for a single junction, (5), is realized with the parameters defined in the Equation (4).

$$\omega_J^2=\frac{2e}{\hbar}\frac{I_c}{C},\quad \tau=\omega_J t,\quad \frac{I_{ext}}{I_c}=i,\ \text{and}\ \gamma=\sqrt{\frac{\hbar C}{2eI_c}}\frac{1}{RC}=(\omega_J RC)^{-1} \tag{4}$$

$$\frac{d^2\phi}{d\tau^2}+\gamma\frac{d\phi}{d\tau}+\sin\phi=i \tag{5}$$

We used the values of γ = 0.7 for the first and third junctions and γ = 1.1 for the middle second junction. Since $\gamma=1/\sqrt{\beta_c}$, the value of γ = 0.7 corresponds to the values of $\beta_c \approx 1.2$ (a different way of writing the Equation (5) would be $\beta_c\frac{d^2\phi}{d\tau^2}+\frac{d\phi}{d\tau}+\sin\phi=i$) that corresponds to approximately 670 - 770 nm feature size junction with the critical current density of $J_c \approx 50$ kA/cm^2 [13]. This critical current density implies that the critical current $I_c=A_J J_c$ ($A_J=\frac{\pi}{4}d^2$) can range approximately from 175 μA to 400 μA for feature size ranged from 670 to O(1000) nm. For lower critical current processes (10 kA/cm^2 and 20 kA/cm^2) values of the critical current will be lower.

The dimensionless equations for an inductively coupled circuit consisting of three inductively coupled Josephson junctions are provided by:

$$\begin{aligned}
&\frac{d^2\phi_1}{d\tau^2}+\gamma_1\frac{d\phi_1}{d\tau}+\sin\phi_1=i_1+\kappa_1(\phi_2-\phi_1)\\
&\frac{d^2\phi_2}{d\tau^2}+\gamma_2\frac{d\phi_2}{d\tau}+\sin\phi_2=i_2+\kappa_1(\phi_1-\phi_2)+\kappa_2(\phi_3-\phi_2)\\
&\frac{d^2\phi_3}{d\tau^2}+\gamma_3\frac{d\phi_3}{d\tau}+\sin\phi_3=i_3+\kappa_2(\phi_2-\phi_3)
\end{aligned} \tag{6}$$

Here $\kappa=\frac{\Phi_0}{2\pi LI_c}$, $\Phi_0=\frac{h}{2e}$ is the magnetic flux quantum, and L is the inductance of the inductor that couples Josephson junctions. The applied current to the junctions includes a DC component and a pulse applied at a certain time for certain duration.

$$i_k(\tau) = i_{DC,k} + \frac{i_{pulse,k}}{\sqrt{2\pi\sigma_k^2}} e^{\frac{-(\tau-\tau_k)^2}{2\sigma_k^2}} \tag{7}$$

The value of the inductance is related to the value of the coupling constant κ according to $L = \frac{L_{J_0}}{\kappa}$ where $L_{J_0} = \frac{\hbar}{2eI_c} = \frac{\Phi_0}{2\pi I_c}$ and will be in the range of $0.83 < L_{J_0} < 1.9\,pH$ for $175 < I_c < 400\,\mu A$. For $\kappa = 0.1$, the characteristic value of the inductance *L* will be approximately $8.3 < L < 19\,pH$.

As we discussed the feature size for a Josephson junction, we would like to briefly discuss the size of the inductor. To estimate the area of the inductor we can employ an approach offered in the reference [14]. Following the reference [14], for state-of-the-art inductor fabrication we can calculate the area of the inductor as $A_L = \frac{L}{l}(\omega + s)$ where L is the inductance, *l* is typical stripline inductance (approximately equal to 0.6 pH/μm), ω is inductor linewidth (approximately 0.35 μm), and *s* is spacing between the inductors (approximately 0.5 μm). Consequently, the area for the inductor will be $12.2 < A_L < 27\,\mu m^2$ for $8.3 < L < 19\,pH$. For practical applications it is very important that area of the memory cell will be small therefore reduction of the inductor size is important. Consequently reduction of the inductor area can be achieved by increasing the value of the coupling constant κ. We have confirmed that a similar memory cell logics can be implemented also for larger values of the coupling constant, for example, κ = 0.5. For κ = 0.5, the values of the inductances will be $1.6 < L < 3.8\,pH$ for $175 < I_c < 400\,\mu A$, and consequently, the area of the inductor will be in the range of $2.4 < A_L < 5.4\,\mu m^2$. Additional reduction of the inductor area may be achieved by even more increasing the value of the coupling constant κ.

In this section we derive the Josephson junction array memory states. We will start with derivation of the potential energy of the entire system. The equation for potential energy of the system, *V*, can be obtained by integrating the right hand sides of Equation (6) with respect to the phases and including the potential energy due to linear inductive coupling between junctions. The function is defined to be zero when all of the phases and their derivatives are zero.

$$V(\phi_1, \phi_2, \phi_3) = \frac{1}{2}\kappa_1(\phi_2 - \phi_1)^2 + \frac{1}{2}\kappa_2(\phi_3 - \phi_2)^2 + 3 + \sum_k(-\phi_k \cdot i_k - \cos\phi_k) \tag{8}$$

Equation (9) shows the derivative of the potential energy function with respect to the three junction phases. A junction phase increase will coincide with the storage or release of energy in the attached inductors. An inductor stores no energy when the phases of the two adjacent junctions are equal. In addition, to increase the phases against the direction of the external currents, work has to be performed. The applied current pulses are omitted for now to investigate the steady states of the system. In equilibrium, each phase resides in a local potential minimum and each of the derivatives is equal to zero.

$$\begin{aligned}
\frac{\partial V}{\partial \phi_1}(\phi_1,\phi_2,\phi_3) &= \kappa_1\phi_1 - \kappa_1\phi_2 - i_{DC,1} + \sin\phi_1 \\
\frac{\partial V}{\partial \phi_2}(\phi_1,\phi_2,\phi_3) &= \kappa_1\phi_2 - \kappa_1\phi_1 + \kappa_2\phi_2 - \kappa_2\phi_3 - i_{DC,2} + \sin\phi_2 \\
\frac{\partial V}{\partial \phi_3}(\phi_1,\phi_2,\phi_3) &= \kappa_2\phi_3 - \kappa_2\phi_2 - i_{DC,3} + \sin\phi_3
\end{aligned} \tag{9}$$

The coupling terms in Equation (8) are the lowest when the phases are relatively close to each other, since the parameters κ_k are usually an order of magnitude smaller than $i_{DC,k}$.

Equilibrium junction phases (junction voltages are equal to zero) can be defined by their offsets θ_k from the negative cosine function's minima, as shown in Equation (10). When adjacent phase differences and external currents are relatively small, the coupling terms will not contribute as much to the potential energy and the phases will have small offsets. The small angle approximation in (11) can then hold.

$$\phi_k = 2\pi n_k + \theta_k \tag{10}$$

$$\left|n_k - n_{k+1}\right| < 3 \quad \Rightarrow \quad \left|\theta_k\right| \le \frac{\pi}{6} \quad \Rightarrow \quad \sin\phi_k \approx \theta_k \tag{11}$$

Applying this relation to Equation (9) and setting the derivatives to zero yields the linearized set of equations, whose solutions θ_k^* estimate the true equilibrium offsets θ_k. Therefore, as long as the phases ϕ_k are near the values of $2\pi n_k$ while system is in equilibrium, their set of offsets θ_k is approximated by the matrix equation in (13).

$$\begin{aligned}
0 &= \kappa_1\left(\theta_1^* + 2\pi n_1\right) - \kappa_1\left(\theta_2^* + 2\pi n_2\right) - i_{DC,1} + \theta_1^* \\
0 &= \kappa_1\left(\theta_2^* + 2\pi n_2\right) - \kappa_1\left(\theta_1^* + 2\pi n_1\right) + \kappa_2\left(\theta_2^* + 2\pi n_2\right) - \kappa_2\left(\theta_3^* + 2\pi n_3\right) - i_{DC,2} + \theta_2^* \\
0 &= \kappa_2\left(\theta_3^* + 2\pi n_3\right) - \kappa_2\left(\theta_2^* + 2\pi n_2\right) - i_{DC,3} + \theta_3^*
\end{aligned} \tag{12}$$

$$\begin{bmatrix} \theta_1^* \\ \theta_2^* \\ \theta_3^* \end{bmatrix} = \begin{bmatrix} \kappa_1 + 1 & -\kappa_1 & 0 \\ -\kappa_1 & \kappa_1 + \kappa_2 + 1 & -\kappa_2 \\ 0 & -\kappa_2 & \kappa_2 + 1 \end{bmatrix}^{-1} \begin{bmatrix} i_{DC,1} - 2\pi\kappa_1\left(n_1 - n_2\right) \\ i_{DC,2} - 2\pi\kappa_1\left(n_2 - n_1\right) - 2\pi\kappa_2\left(n_2 - n_3\right) \\ i_{DC,3} - 2\pi\kappa_2\left(n_3 - n_2\right) \end{bmatrix} \tag{13}$$

For the sake of simplicity, in this paper we consider the case of equal coupling values, $\kappa_1 = \kappa_2 = \kappa$, and opposite currents applied to the junctions on the ends, $i_{DC,1} = -\, i_{DC,3}$. Equation (14) shows the results of Equation (13) given the constraints on the parameters and the following definitions: $d_{12} = n_1 - n_2$, $d_{23} = n_2 - n_3$.

$$\begin{aligned}
\theta_1^* &= \frac{1}{\kappa+1} i_{DC,1} + \frac{\kappa}{3\kappa+1} i_{DC,2} + \frac{-2\pi\kappa\left(2\kappa+1\right)}{3\kappa^2+4\kappa+1} d_{12} + \frac{-2\pi\kappa^2}{3\kappa^2+4\kappa+1} d_{23} \\
\theta_2^* &= 0 \cdot i_{DC,1} + \frac{\kappa+1}{3\kappa+1} i_{DC,2} + \frac{2\pi\kappa}{3\kappa+1} d_{12} + \frac{-2\pi\kappa}{3\kappa+1} d_{23} \\
\theta_3^* &= \frac{-1}{\kappa+1} i_{DC,1} + \frac{\kappa}{3\kappa+1} i_{DC,2} + \frac{2\pi\kappa^2}{3\kappa^2+4\kappa+1} d_{12} + \frac{2\pi\kappa\left(2\kappa+1\right)}{3\kappa^2+4\kappa+1} d_{23}
\end{aligned} \tag{14}$$

Sets of steady state phase offsets, normalized by 2π, are presented in the Table 1. The driving currents are $i_{DC,1} = 1.0$, $i_{DC,2} = 0.8$, $i_{DC,3} = -1.0$ and the coupling parameters are $\kappa_1 = \kappa_2 = 0.1$. The Table includes all of the possible sets of steady state offsets where $n_1 \geq n_2 \geq n_3$ and $n_1 - n_3 \leq 2$. Without loss of generality, n_3 is defined to be 0 since the locations of local minima are symmetric to shifting all phases by 2π. For simplicity, we only present in Table 1 the states for $n_j < 3$. The estimated offsets θ_k^* found from (14) are rather close (within ~17°) of the numerical solutions θ_k found from minimization via the Nelder-Mead simplex (direct search) method on the potential function. The final column shows the values of the potential function at the local minima.

n_1	n_2	n_3	$\theta_1^*/2\pi$	$\theta_2^*/2\pi$	$\theta_3^*/2\pi$	$\theta_1/2\pi$	$\theta_2/2\pi$	$\theta_3/2\pi$	V
0	0	0	0.1545	0.1077	–0.1349	0.1992	0.1187	–0.1552	–1.272
1	0	0	0.0706	0.1847	–0.1279	*no stable minimum*			--
1	1	0	0.1475	0.0308	–0.0510	0.1810	0.0338	–0.0515	–9.918
2	0	0	–0.0134	0.2616	–0.1209	*no stable minimum*			--
2	1	0	0.0636	0.1077	–0.0440	0.0661	0.1164	–0.0437	–14.05
2	2	0	0.1405	–0.0461	0.0329	0.1670	–0.0443	0.0333	–15.29

Table 1: The offset phases of local minima of the potential function V in Equation (8), when $i_{DC,1} = 1.0$, $i_{DC,2} = 0.8$, $i_{DC,3} = -1.0$, $\kappa_1 = \kappa_2 = 0.1$. Each row shows the approximated offset phases from Equation (13), θ_k^*, and the true offset phases of the local minima, θ_k, for a given set of the multiples of 2π phase differences, n_k. All of the offset phases (in radians) are scaled by 2π. The last column provides the potential value V at the local minima.

For the set of DC currents and coupling parameters, no steady state set exists when the first junction phase is about 2π greater than both of the other two junction phases (see rows where $\{n_1,n_2,n_3\}=\{1,0,0\}$ and $\{2,0,0\}$). As will be discussed further in the next section, the lack of these stable states is crucial to the memory cell design since for memory cell demonstration we are only interested in manipulating the system within a particular sets of states, namely states $\{0,0,0\}$ and $\{1,1,0\}$ in the highlighted rows of the Table 1.

The set of states $\{n_1,n_2,n_3\}$ listed in Table 1 shows equilibrium phases for the specific set of driving currents $i_{DC,1} = 1.0$, $i_{DC,2} = 0.8$, $i_{DC,3} = -1.0$. If any of these currents were to change slightly, the equilibrium phases would adjust accordingly, but still reside in the same potential wells described by n_k. When the values of the currents change significantly, some of these steady states become unstable and no longer exist.

Figure 2 shows state $\{n_1,n_2,n_3\}$ existence intervals as a function of the values of the first junction DC current values $i_{DC,1}$ while keeping the values of the other junction currents fixed. Figures 3 and 4 show state existence intervals as functions of the DC current applied to the second and the third junction, respectively. The right plots show enlarged views of intervals of state existence curves near the parameter values that we will be using for memory operations. These are identified by the vertical dashed lines.

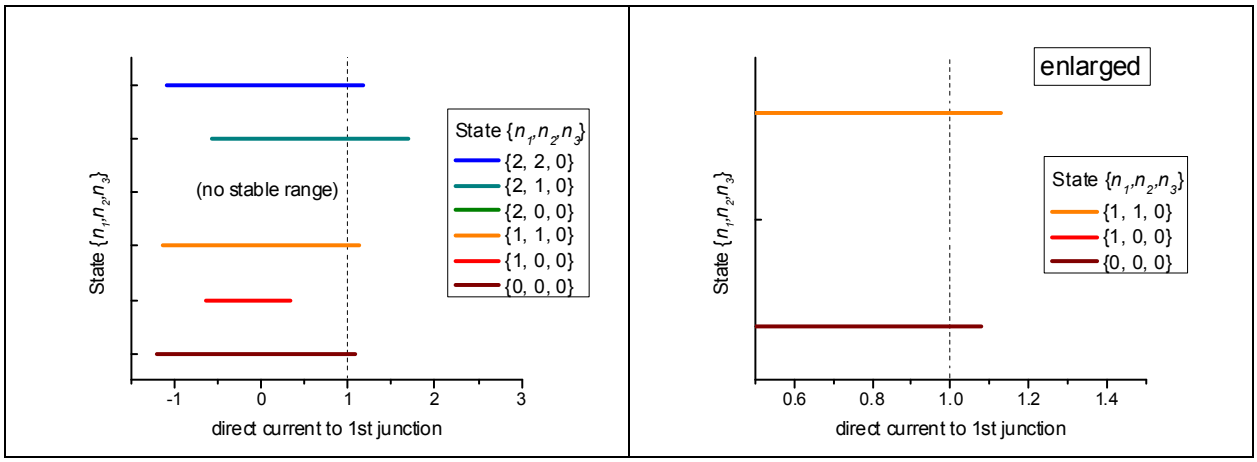

Figure 2: The ranges of stability for the available states as a function of $i_{DC,1}$. $i_{DC,2}$ = 0.8, $i_{DC,3}$ = −1.0. The vertical dashed line shows the default value of $i_{DC,1}$ = 1.0. The right plot shows a partial set of states.

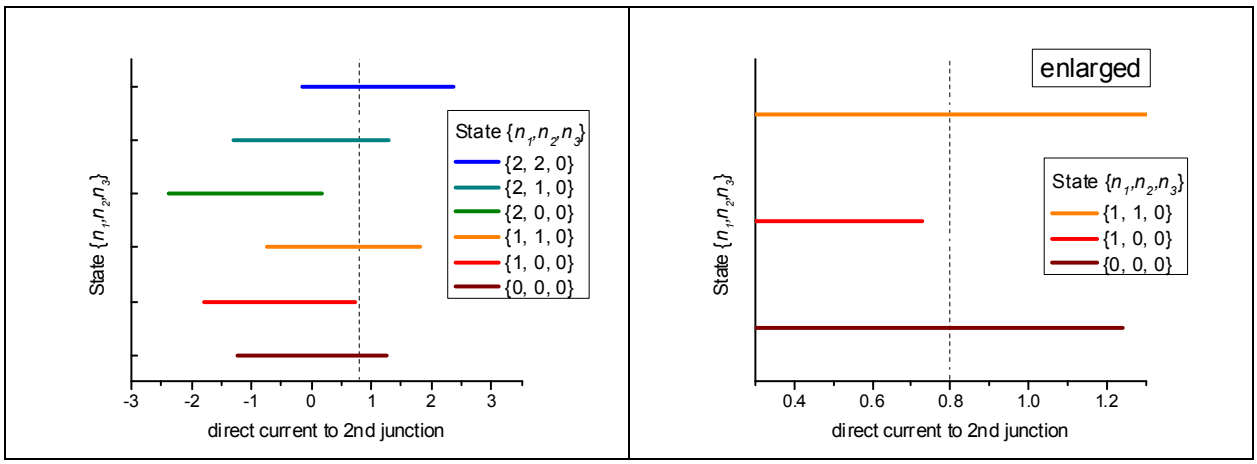

Figure 3: The ranges of stability for available states as a function of $i_{DC,2}$. $i_{DC,1}$ = 1.0, $i_{DC,3}$ = −1.0. The vertical dashed line shows the default value of $i_{DC,2}$ = 0.8. The right plot shows a partial set of states.

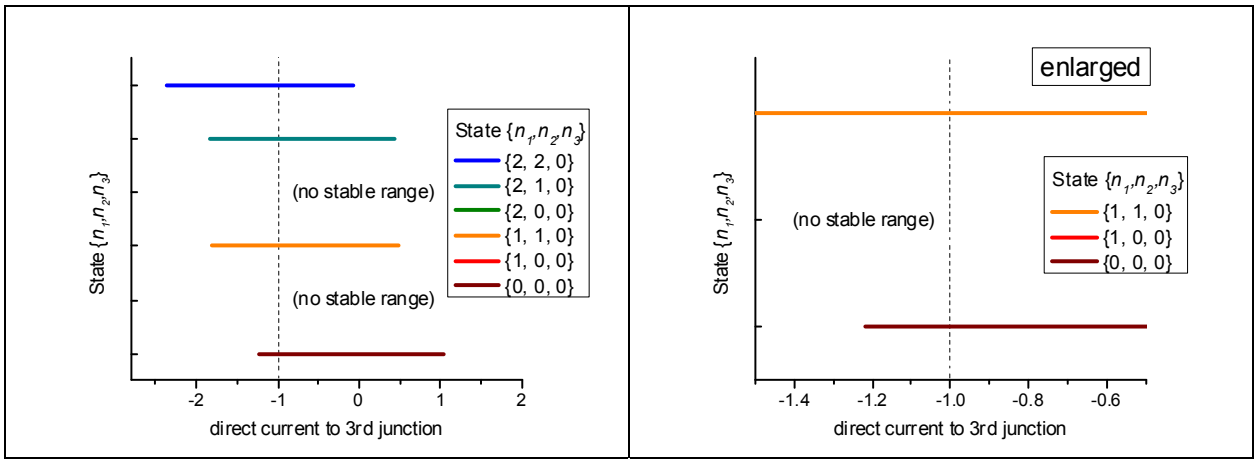

Figure 4: The ranges of stability for available states as a function of $i_{DC,3}$. $i_{DC,1}$ = 1.0, $i_{DC,2}$ = 0.8. The vertical dashed line shows the default value of $i_{DC,3}$ = −1.0. The right plot shows a partial set of states.

These stability diagrams are used in defining the values of DC currents for memory operations. Adequately choosing parameter values and states to consider for memory operations is very important

since many options are available. In this paper we do not perform rigorous optimization studies to optimize parameters for memory operation (optimization studies are presented in the following paper). We note that junction currents where states partially (not fully) overlap may be chosen as a possible candidate for memory operation. Operating the circuit with the current values that are at the edges of the state overlap may show the highest robustness to the applied Write and Read pulses. Such memory operations are demonstrated later in the paper.

Memory Access Times and Energies

In this section we will describe the dynamics of the circuit and will calculate the access times of circuit response to current pulses, which constitute memory Write, Read, and Reset operations. The dynamics of the array is described by Equations (6). Our numerical results and mathematical analysis show that, in the limit of weak coupling strength (possibly weak-to-moderate coupling), pulse operation to a single junction induces separable dynamics where only one junction moves significantly at a given time while the rest of the junctions are close to their steady state positions (examples of such separable behavior are presented in the next Section where we present examples of memory operations). This conclusion is also consistent with the previously published work [14, 15]. To study the dynamics of the array, we first rewrite Equations (6) in the following form (Equation (15)).

$$\begin{aligned}
\gamma_1 \frac{d\phi_1}{d\tau} &= i_1 + \kappa_1(\phi_2 - \phi_1) - \sin\phi_1 \\
\gamma_2 \frac{d\phi_2}{d\tau} &= i_2 + \kappa_1(\phi_1 - \phi_2) + \kappa_2(\phi_3 - \phi_2) - \sin\phi_2 \\
\gamma_3 \frac{d\phi_3}{d\tau} &= i_3 + \kappa_2(\phi_2 - \phi_3) - \sin\phi_3
\end{aligned} \tag{15}$$

We neglect the contribution of the second derivative since for the regimes of our consideration it is rather small relative to the first derivative. Since all the coupling terms are equal, we can rewrite these equations in the following way.

$$\begin{aligned}
\gamma_1 \frac{d\phi_1}{d\tau} &= i_1 + \kappa(\phi_2 - \phi_1) - \sin\phi_1 \\
\gamma_2 \frac{d\phi_2}{d\tau} &= i_2 + \kappa(\phi_1 - 2\phi_2 + \phi_3) - \sin\phi_2 \\
\gamma_3 \frac{d\phi_3}{d\tau} &= i_3 + \kappa(\phi_2 - \phi_3) - \sin\phi_3
\end{aligned} \tag{16}$$

Due to separable motion of each junction (only one junction moves at a given time), Equations (16) can be decoupled and rewritten in the following form.

$$\begin{aligned}
\gamma_1 \frac{d\phi_1}{d\tau} &= i_1 + \kappa(\phi_{2eq} - \phi_1) - \sin\phi_1 \\
\gamma_2 \frac{d\phi_2}{d\tau} &= i_2 + \kappa(\phi_{1eq} + 2\pi - \phi_2) - \kappa(\phi_2 - \phi_{3eq}) - \sin\phi_2 \\
\gamma_3 \frac{d\phi_3}{d\tau} &= i_3 + \kappa(\phi_{2eq} + 2\pi - \phi_3) - \sin\phi_3
\end{aligned} \tag{17}$$

Here ϕ_{1eq}, ϕ_{2eq}, ϕ_{3eq} are the equilibrium phases of the junctions. The mathematical basis for the solution of these equations was presented in [15, 16]. However, we would like to clarify that while in the Braiman et

al. papers all the junctions were driven and the steady solution constituted to the nonzero voltage (velocity), in this paper we only drive one junction for a short period of time. We are only interested in one period of integration that is required for the array to respond to external pulse applied to that single junction. Subsequently, in the time between the pulse excitations required for memory operations, junctions' voltages are zeros. We also approximate pulse shape for excitation as rectangular. Taking into consideration all the approximations presented above, for the reason of completeness and clarity, we are following derivations from the reference [15]. We first write these equations in a rather generic form:

$$\gamma \frac{d\phi}{dt} = F(\phi) \tag{18}$$

and

$$dt = \gamma \frac{d\phi}{F(\phi)} \tag{19}$$

Subsequently,

$$T = \gamma \int \frac{d\phi}{F(\phi)} = \gamma \int d\phi \exp(-\ln(F(\phi)) \tag{20}$$

We can now expand

$$\ln F(\phi) \approx \ln(\mathrm{F}(\phi_c)) + \frac{F'}{F}(\phi - \phi_c) + \frac{FF'' - F'^2}{2F^2}(\phi - \phi_c)^2 + \ldots \tag{21}$$

Since $F'(\phi_c) = 0$, we get

$$\ln F(\phi) \approx \ln(\mathrm{F}(\phi_c)) + \frac{F''(\phi_c)}{2F(\phi_c)}(\phi - \phi_c)^2 + \ldots \tag{22}$$

Using saddle-point integration method, we obtain

$$T \approx \gamma F^{-1}(\phi_c) \int_{-\infty}^{\infty} \exp(-(\frac{F''(\phi_c)}{2F(\phi_c)}(\phi - \phi_c)^2) d\phi \tag{23}$$

or

$$T \approx \gamma F^{-1}(\phi_c) \sqrt{\frac{2\pi F(\phi_c)}{F''(\phi_c)}} = \gamma \sqrt{\frac{2\pi}{F(\phi_c)F''(\phi_c)}} \tag{24}$$

For each junction we will use a subscript to describe the particular *F*.

$$\begin{aligned} F_1(\phi_1) &= i_1 + \kappa(\phi_{2eq} - \phi_1) - \sin\phi_1 \\ F_2(\phi_2) &= i_2 + \kappa(\phi_{1eq} + 2\pi - \phi_2) - \kappa(\phi_2 - \phi_{3eq}) - \sin\phi_2 \\ F_3(\phi_3) &= i_3 + \kappa(\phi_{2eq} + 2\pi - \phi_3) - \sin\phi_3 \end{aligned} \tag{25}$$

In our setup, $i_{3dc} = -i_{1dc}$, thus

$$F_3(\phi_3) = -i_{1dc} + i_{3\,pulse} + \kappa(\phi_{2eq} + 2\pi - \phi_3) - \sin\phi_3 \tag{26}$$

Also for very small values of the coupling κ, $\phi_c \approx \pi/2$ therefore we rewrite the expressions for functions F as

$$\begin{aligned} F_1(\phi_c) &= i_1 + \kappa(\phi_{2eq} - \pi/2) - 1 \\ F_2(\phi_c) &= i_2 + \kappa(\phi_{1eq} + 2\pi - \pi/2) - \kappa(\pi/2 - \phi_{3eq}) - 1 \\ F_3(\phi_c) &= i_3 + \kappa(\phi_{2eq} + 2\pi - \pi/2) - 1 \end{aligned} \tag{27}$$

Since second derivative of F is equal to $\sin(\phi_c) \approx 1$, this term can now be omitted. Thus we get

$$\begin{aligned} T_1 &\approx \gamma\sqrt{\frac{2\pi}{i_1 + \kappa(\phi_{2eq} - \pi/2) - 1}} \\ T_2 &\approx \gamma\sqrt{\frac{2\pi}{i_2 + \kappa(\phi_{1eq} + 2\pi - \pi/2) - \kappa(\pi/2 - \phi_{3eq}) - 1}} \\ T_3 &\approx \gamma\sqrt{\frac{2\pi}{i_3 + \kappa(\phi_{2eq} + 2\pi - \pi/2) - 1}} \end{aligned} \tag{28}$$

We can estimate the values of the time (period T) required to complete the transition from one state to another (which is, in principle, the time delay between the application of the pulse to the circuit response).

$$\begin{aligned} T_1 &\approx \gamma\sqrt{\frac{2\pi}{i_1 + \kappa(\phi_{2eq} - \pi/2) - 1}} \approx \gamma\sqrt{\frac{2\pi}{i_1 + \kappa(2\pi \times 0.15 - \pi/2) - 1}} \approx \gamma\sqrt{\frac{2\pi}{i_{pulse} - 0.2\kappa\pi}} \approx 6.25 \approx 26\,ps \\ T_2 &\approx \gamma\sqrt{\frac{2\pi}{i_2 + \kappa(\phi_{1eq} + 2\pi - \pi/2) - \kappa(\pi/2 - \phi_{3eq}) - 1}}_2 \\ &\approx \gamma\sqrt{\frac{2\pi}{i_2 + \kappa(\phi_{1eq} + 2\pi - \pi/2) - \kappa(\pi/2 - \phi_{3eq}) - 1}} \approx 6.5 \approx 27\,ps \\ T_3 &\approx \gamma\sqrt{\frac{2\pi}{i_3 + \kappa(\phi_{2eq} + 2\pi - \pi/2) - 1}} \approx \gamma\sqrt{\frac{2\pi}{i_3 + \kappa(\phi_{2eq} + 2\pi - \pi/2) - 1}} \approx 3 \approx 12\,ps \end{aligned} \tag{29}$$

The time periods in Equations (29) provide a fair estimation of the access times for memory operations (memory operations can be applied to any junction and in the following section we will provide examples of memory operation). Our numerical results show similar access times thus our estimation is that access times for the entire operation (including reset times) will stay in the range of 50-100 ps.

We would like to briefly discuss junction switching and dissipation energies required for basic memory cell operations. Resistively shunted junction (RSJ) potential energy can be written as: $E(\varphi) = E_J(1 - \cos\varphi - \frac{I_b}{I_c}\varphi)$ where I_b is bias current, I_c is critical current and $E_j = I_c\Phi_0/(2\pi)$. The

energy difference between the two minima is given by $\Delta E = 2\pi \frac{I_b}{I_c} E_J$. The switching energy is equal to the height of the potential barrier between the adjacent minima which is $\Delta E = 2\pi \frac{I_b}{I_c} E_J = 2\pi \frac{I_b}{I_c} \frac{I_c \Phi_0}{2\pi} = I_b \Phi_0$. Consequently, the switching energy for a "conventional" SFQ process theoretically can be very low provided that the bias current is low. This is not the case in typical experiments and typical value of the bias current due to circuit speed and error bit optimization process is $I_b = 0.7 I_c$ [14] that make switching energy equal to about $1.4 \times 10^{-19} J$.

For a design based on coupled arrays of Josephson junction's logics, the switching energy can also be arbitrarily small and is equal to $\Delta E = I_{pulse} \Phi_0$ where I_{pulse} is pulse current. For very small pulses however one could may run into the same issues as for a "conventional" switching process. If I_{pulse} is very small robustness and stability of memory operation may be compromised due to disorder, noise, and other reasons. For that same reason in our simulations the switching energy was also in the range of 5×10^{-18} - 10^{-19} J.

Perhaps a much more important parameter in memory cell operation would be energy loss/dissipation per bit of operation. Energy dissipation for one flip is given by the same expression as the expression for flipping energy $I_b \Phi_0$. Energy dissipation is one of major issues for superconducting computing [10]. For RSFQ cells the average number of Josephson junction switches per bit operation is in the range of 10 [14]. Since in the proposed design all major memory cell operation (Read, Write, Reset) are implemented on the same circuit, the number of switching per bit could be reduced. For the proposed logics, only one or two junctions have to be switched in order to implement any of the basic memory operations. This could potentially indicate on a benefit using array-based memory cell logics.

Memory Cell Operation

In this Section we will present basic memory cell operations (Write, Read, and Reset). A circuit can operate as a memory cell if a set of operators can transition the system to well-defined states and can output a signal that discriminates memory states. The value n_k, as presented in Equation (10), will describe the location of the k^{th} junction phase. When all three junction phases are in the same sinusoidal potential well, the system will be considered in the '0' state, $\{n_1,n_2,n_3\} = \{0,0,0\}$. When the phases of the first and second junctions are shifted to the next potential well (about 2π greater), the cell will be in the '1' state, $\{n_1,n_2,n_3\} = \{1,1,0\}$. These two states correspond to the first and third rows of Table 1, highlighted in gray.

The proposed circuit (see Figure 1) or family of similar circuits can be employed in variety of ways to implement a functional memory device. Here we are demonstrating just one example of basic memory operation and we only use two states as '0' and '1'. We would like to note that memory operations presented below may not be the optimal for this circuit and additional studies are required to optimize memory cell operation designs. We will be employing Gaussian pulses to demonstrate memory cell logics however other types of pulses (such as squire pulse, single flux quanta (SFQ), or other shapes) can be used as well.

The presented memory cell logics are fundamentally different from the conventional single flux quanta (SFQ) logics. An SFQ pulse is a voltage pulse generated at the Josephson junction when the phase difference for a junction flip is exactly 2π. Josephson relation $\frac{d\varphi}{dt} = \frac{2e}{\hbar} V$ guarantees then that SFQ

pulses have a quantized area equal to a single flux quantum $\int V dt = \frac{\hbar}{2e}\int_0^{2\pi}\frac{d\varphi}{dt}dt = \frac{h}{2e} \equiv \Phi_0$ that is a single flux quantum. Since in our presented memory cell design, memory states are generated and recorded based on the array dynamics, junction phase rotations are not equal exactly to 2π or its multiples.

Write '1' Operation

If a pulse applied to the system always yields a transition to the '1' state, then the operation can be considered as a memory Write '1' operation. The equilibrium configuration of the phases in the '1' state is a stable state where the phases of the first and second junction are shifted into the next potential well (approximately 2π greater than the phase of the third junction). In order for the transition from the '0' state to the '1' state to be successful, the energy injected into the system by a pulse must only affect the phases of the first and second junctions. In our example design, we apply a pulse to the first junction. Due to the coupling between the first and second junctions, this pulse will cause to the phase shift of the second junction as well. The potential energy of state '1' is less than the potential energy of state '0'. The phase of the third junction will not change for the choice of system and pulse parameters.

The curves in Figure 5 show the response to the Gaussian pulse of size $i_{pulse,1} = 1.0$ being applied to the first junction after the system has settled into its '0' state. All of the pulses described in this section will have a pulse width of 0.1 and a pulse center at zero time. The phase dynamics shown in Figure 5 show the phase of the first junction rising quickly to the next local minimum, followed by the phase of the second junction. The phase of the third junction slightly shifts its equilibrium position but stays in the same potential well. The period of the full transition from states '0' to '1' is of the order of 25 units of time, which is the equivalent of 100 ps. The slower time scale is due to the fact that the system undergoes two transitions. The energy per pulse is of the order of 5×10^{-19} J. This energy is very typical for any other memory command pulses. After the excitation, junction phases begin to slow down near the state $\{n_1,n_2,n_3\} = \{1,0,0\}$, but since no local minimum exists there phases then start a second transition to state '1' at $\{n_1,n_2,n_3\} = \{1,1,0\}$.

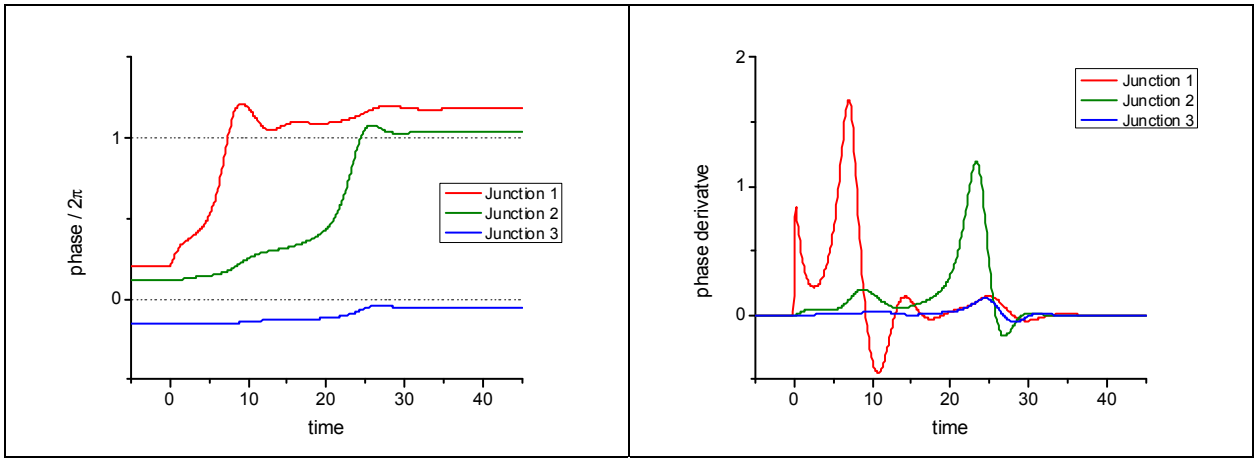

Figure 5: The time dependences of phases scaled by 2π (left) and phase derivatives (right) of the system in response to a Gaussian pulse applied to the first junction when the system is in state '0'. $i_{pulse,1} = 1.0$.

Figure 6 shows the responses of first junction phase as a function of time for a variety of pulse amplitudes. The pulse widths σ are all fixed at 0.1, but the amplitudes range from 0.5 to 1.5 (see Equation (7) for the definition of the Gaussian pulse).

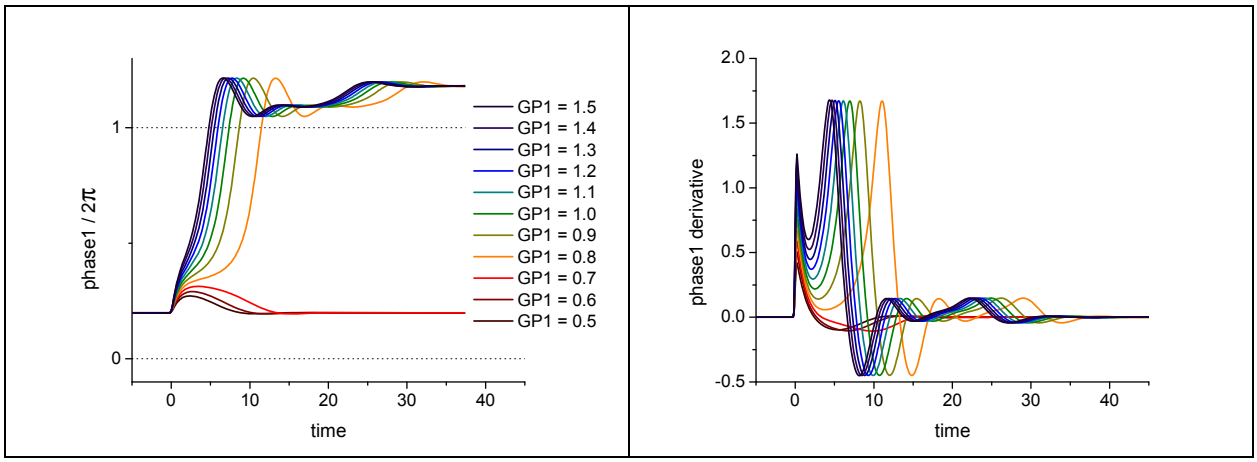

Figure 6: The time series of the first junction phase scaled by 2π (left) and first junction phase's derivative (right) of the system in response to a Gaussian pulse applied to the first junction when the system is in state '0'. The pulse amplitudes $i_{pulse,1}$ go from 0.5 (dark red) to 1.5 (dark violet).

The pulses add energy into the system. If this energy is sufficient to overcome the barrier energy, then the system transitions into the steady state corresponding to state '1'. The maximum value of the derivative of the phase is as high as 1.6, which is the equivalent of 0.8 mV. The large derivative magnitude is caused by the 2π phase slip. Its peak stays around 1.6 independent of the size of the pulse that triggered it.

The barrier energy is illustrated in Figure 7. It shows the potential energy of the system over time for the responses plotted in Figure 6. Most of the curves show potential energy increase and then rapidly decrease after passing the energy barrier. The three curves where pulse values $i_{pulse,1}$ are less than 0.8 fail to pass beyond the potential threshold and consequently do not transition to the next state. The barrier energy found from this figures is about 0.045, which is the equivalent of 10^{-19} J or 0.1 aJ.

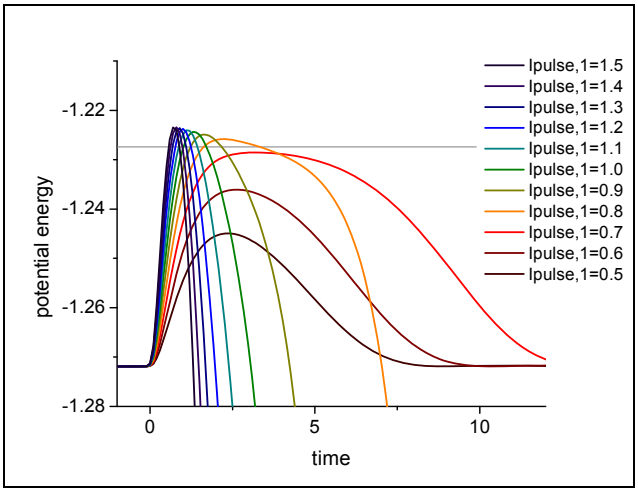

Figure 7: The time series of the system's potential energy of the responses shown in Figure 6. The Gaussian pulse amplitudes $i_{pulse,1}$ vary from 0.5 (dark red) to 1.5 (dark violet). The barrier energy is around 0.045. The gray line shows the sum of the initial potential energy and the barrier energy.

If the same pulse (as the one in Figure 5) is applied to the first junction when the system is already in state '1', as shown in Figure 8, no change to the relative phase differences occurs (after the transient dynamics dissipate). The system remains in state '1'. Therefore, this pulse can be interpreted as a Write '1' operator since the final state will always be '1' after it is applied to either initial steady state.

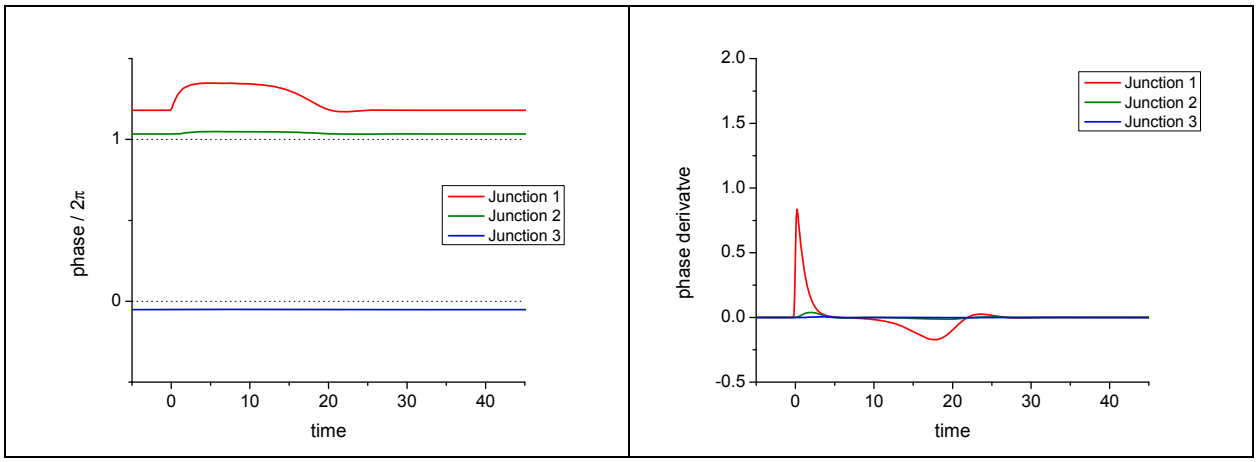

Figure 8: The time series of phases scaled by 2π (left) and phase derivatives (right) of the system in response to a Gaussian pulse applied to the first junction when the system is in state '1'. $i_{pulse,1}$ = 1.0.

Another criterion for the first pulse's amplitude must be noted: it cannot be strong enough to drive the system out of state '1'. In Figure 9 we demonstrate the time dependent responses of the first junction phase to a set of pulses with variable strengths. If the pulse is strong enough, it will transition the circuit from state '0' to '1'. Strong enough pulses that exceed the energy barrier will drive the circuit from the state $\{n_1,n_2,n_3\}$ = {1,1,0} to the state $\{n_1,n_2,n_3\}$ = {2,1,0}. These pulses are unacceptably strong.

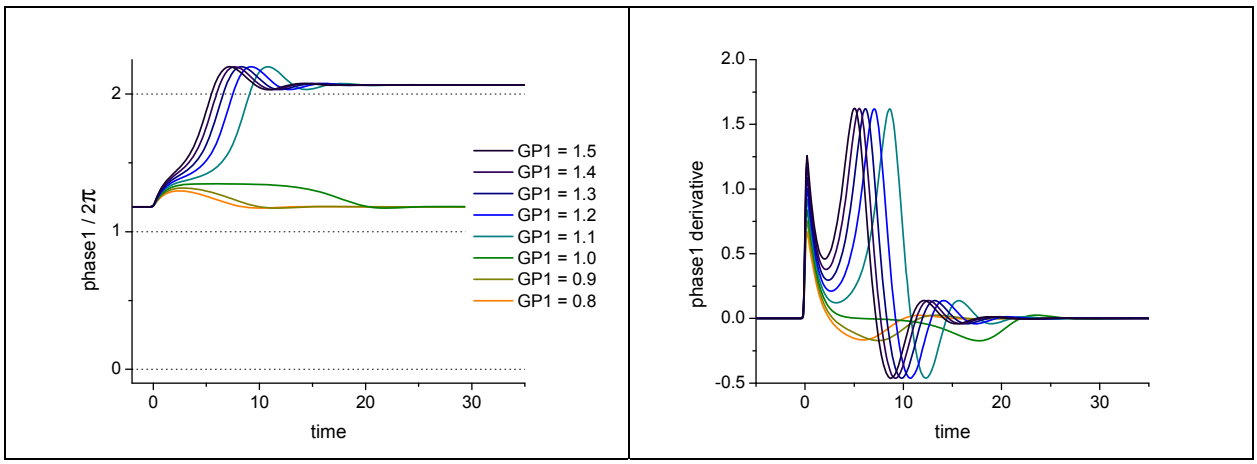

Figure 9: The time series of first junction phase scaled by 2π (left) and first junction phase's derivative (right) of the system in response to a Gaussian pulse applied to the first junction when the system is in state '1'. The pulse amplitudes $i_{pulse,1}$ vary from 0.8 (yellow) to 1.5 (dark violet).

Write '0' Operation

The memory's Write '0' or Reset operation is implemented by sending a pulse to the third junction. The transition from state '1' back to '0' is demonstrated in Figure 10 where the pulse applied to the third junction has an amplitude of $i_{pulse,3}$ = 5.0. After the third junction phase moves one potential well, all the phases are within the same potential well (i.e. have the same multiple of 2π). The new steady state phases are exactly 2π larger than the phases in the {0,0,0} state. The new state is $\{n_1,n_2,n_3\}$ = {1,1,1}, which by definition is equivalent to state {0,0,0}. The transformation occurs over a similar time period that was calculated according to the approximation calculated in Equation (29).

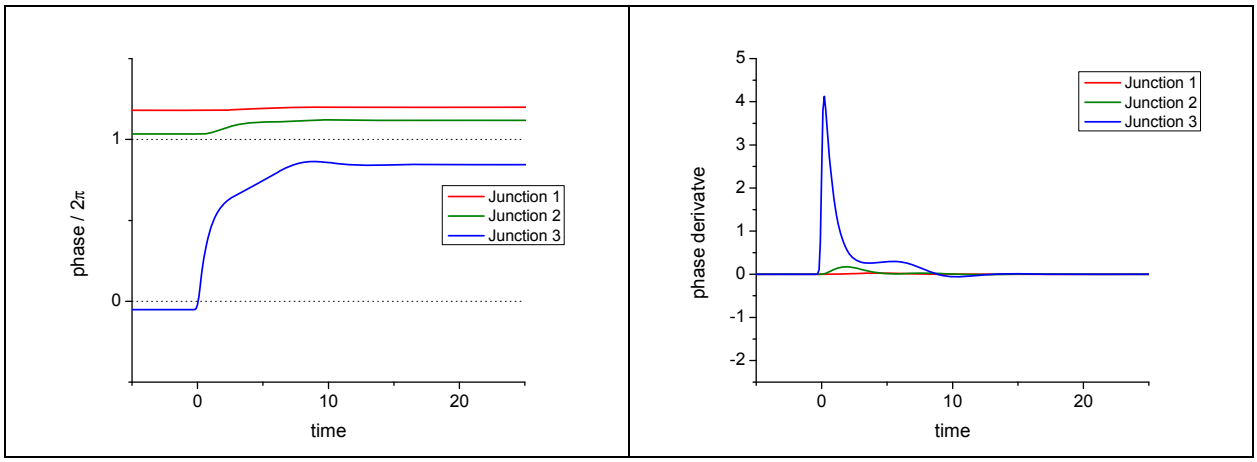

Figure 10: The time series of phases scaled by 2π (left) and phase derivatives (right) of the system in response to a Gaussian pulse applied to the third junction when the system is in state '1'. $i_{pulse,3}$ = 5.0.

For this pulse to successfully reset the state from '1' to '0', the pulse needs to be strong enough to counter the driving current in the opposing direction. This is why this pulse's amplitude is greater than that of the Write "1" pulse. Figure 11 shows the responses of the system in state '1' to a collection of pulses applied to the third junction whose amplitudes $i_{pulse,3}$ range from 4.5 to 5.2. Only the pulse amplitudes equal to 4.9 and larger are sufficient to let the system exceed the potential threshold. The derivative of the third phase increases up to a value of 4.5, which is the equivalent of 2.25mV.

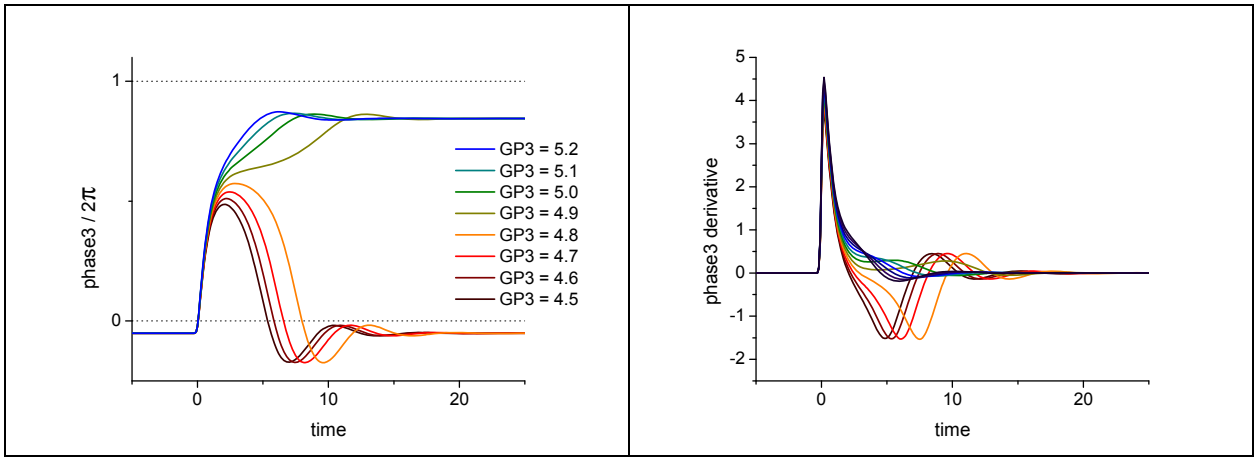

Figure 11: Time series of the third junction phase scaled by 2π (left) and third junction phase's derivative (right) of the system in response to a Gaussian pulse applied to the third junction when the system is in state '1'. The pulse amplitudes $i_{pulse,3}$ vary from 4.5 (dark red) to 5.2 (blue).

To analytically estimate the barrier energy of this transition, a simplified description of the dynamics is used. The response is assumed to be the transition of the third junction phase while the phases of other junctions remain in their positions. The potential function would then become Equation (30).

$$V\left(\phi_3 \middle| \phi_1 = \phi_2 = 2\pi\right) = \frac{\kappa_2}{2}\left(\phi_3 - 2\pi\right)^2 - i_{DC,3} \cdot \phi_3 - \cos\phi_3 - 2\pi\left(i_{DC,1} + i_{DC,2}\right) + 1 \qquad (30)$$

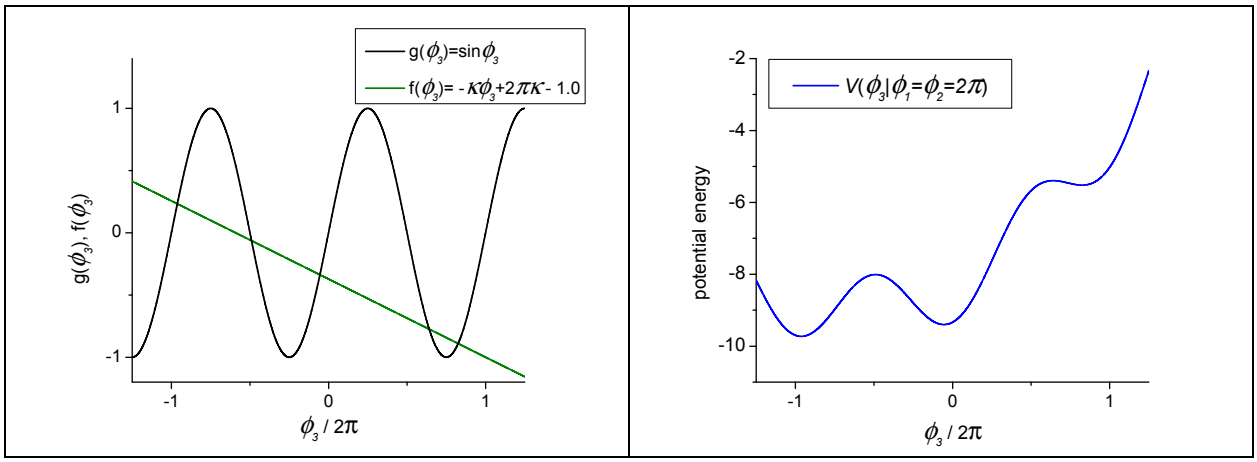

Figure 12 The left figure compares the functions on the left (green) and right (black) sides of Equation (31), where $i_{DC,3}$ = 1 and κ_2 = 0. The right figure shows the potential energy V as a function of the third junction phase when the other junction phases are fixed at 2π. Intersections in the left plot correspond to local extrema in the right plot. The barrier energy between the minima near ϕ_3 = 0 and ϕ_3 = 2π is 4.00.

The local minimum and maximum would occur when ϕ_3 satisfies Equation (31), which equates a linear function with a sine function. These two functions are plotted in Figure 12(left) for the set of parameters as defined above. The corresponding potential as a function of the third junction phase, Equation (30), is plotted in Figure 12(right). The intersections of the left plot correspond to local extrema on the right plot. The difference in potential between the minimum near 0 and the maximum before 2π is 4.00, the estimated barrier energy using the simplified description of the dynamics.

$$\phi_3 \text{ of local extrema of } V, \text{ when } \phi_1 = \phi_2 = 2\pi: \quad -\kappa_2\phi_3 + 2\pi\kappa_2 + i_{DC,3} = \sin\phi_3 \tag{31}$$

For the system to switch its steady state, the gain in potential energy of the circuit due to the pulse must increase by the amount equal to the barrier energy (3.81 in dimensionless units), as shown in Figure 13 that pictures the potential energies of the system as functions of time for the responses to the pulses shown in Figure 13. The barrier energy found by solving the simplified equations in Equations (30) and (31) would indicate that none of the responses plotted are viable.

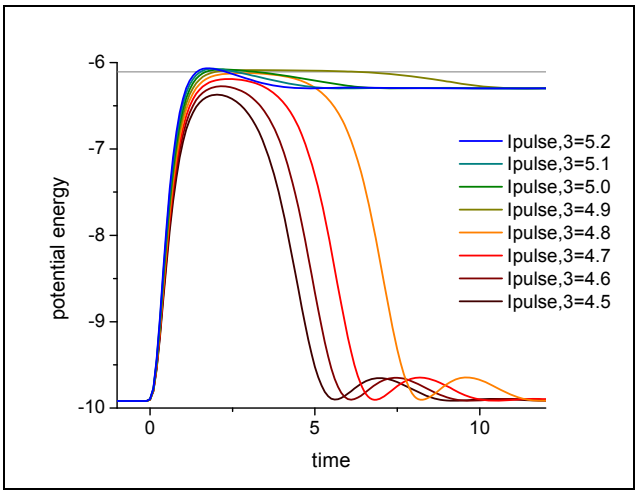

Figure 13: The time series of the system's potential energy of the responses shown in Figure 11. The Gaussian pulse amplitudes $i_{pulse,3}$ vary from 4.5 (dark red) to 5.2 (blue). The barrier energy is around 3.81. The gray line shows the initial potential energy plus the barrier energy.

Figure 14 shows the response of the same pulse as the one in Figure 11 when the junction array state is '0'. No change in the state is observed after the transient behavior dissipates. This pulse will send the

system into state ‘0’ from either initial state. This suggests that the pulse applied to the third junction can be used as a Write ‘0’ operation.

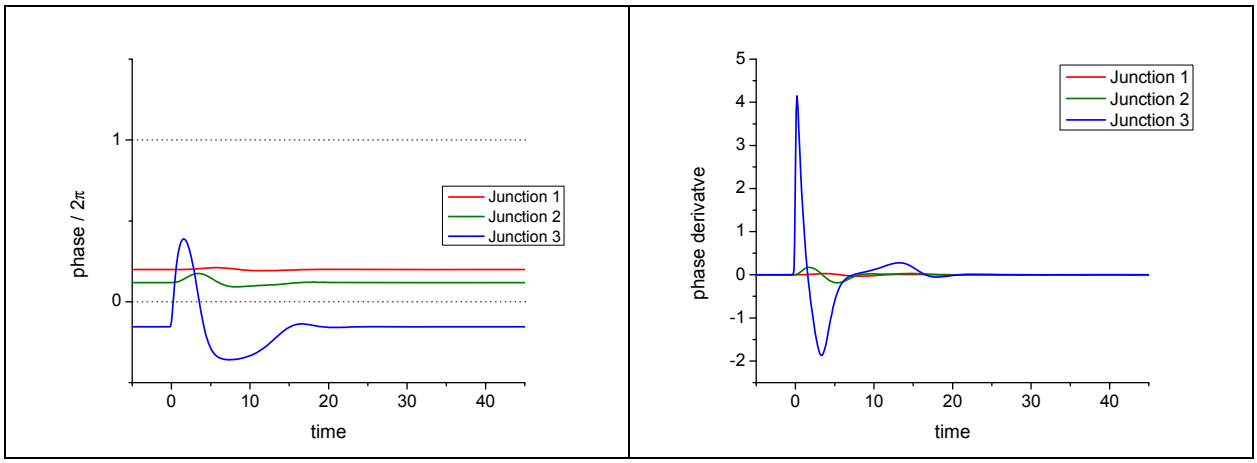

Figure 14: The time series of phases scaled by 2π (left) and phase derivatives (right) of the system in response to a Gaussian pulse applied to the third junction when the system is in state ‘0’. $i_{pulse,3}$ = 5.0.

Since the third junction’s forcing term is in the opposite direction to the first junction’s forcing term, the potential energy profile as a function of only the third junction has a different sign of its slope. Figure 15 shows that if a pulse is too strong, it would provide too much kinetic energy to the third junction and the system would transition over the potential barrier in the opposite direction. This third junction phase would settle into a steady state that is different from the other junction phases by approximately a multiple of 2π. This would be the state $\{n_1,n_2,n_3\} = \{0,0,-1\} = \{1,1,0\}$. The figures show the responses of the system in state ‘0’ to a set of pulses applied to the third junction whose amplitudes $i_{pulse,3}$ range from 4.5 to 5.5.

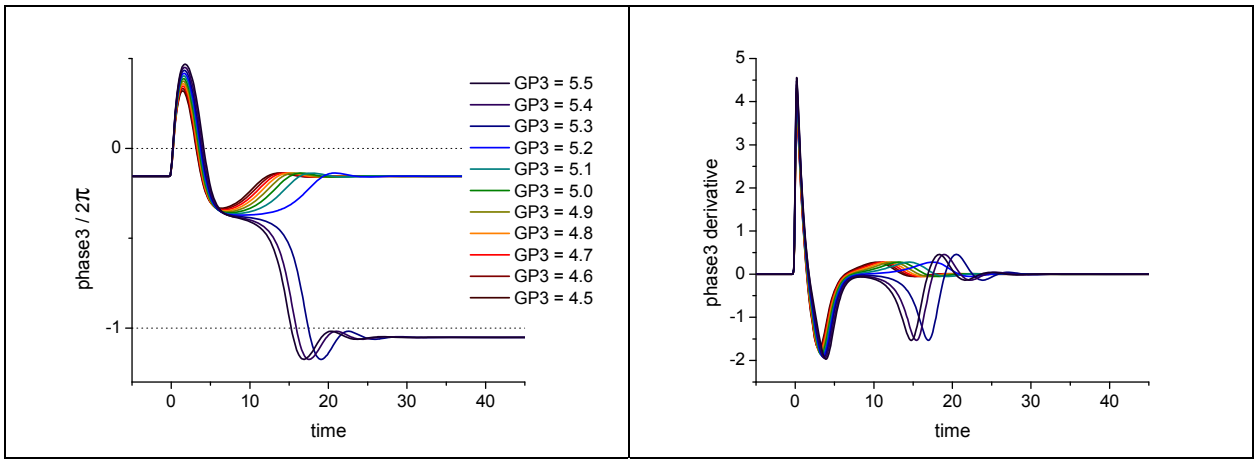

Figure 15: The time series of the third junction phase scaled by 2π (left) and third junction phase’s derivative (right) of the system in response to a Gaussian pulse applied to the third junction when the system is in state ‘0’. The pulse amplitudes $i_{pulse,3}$ go from 4.5 (dark red) to 5.5 (dark violet).

Read Operation

In order to read the memory state, we use a pulse that can be applied to one of the junctions. A condition of a successful Read operation is that application of a Read pulse results in different outputs from the circuit dependent on whether the circuit was at the ‘0’ or ‘1’ memory state. The same pulse that we use for the Write ‘1’ operation, applied to the first junction, can serve as our Read command. The Read data will be taken from the voltage response of the second junction. When the initial state of the circuit is ‘1’, there will be almost no response of the second junction phase to the applied pulse. On the contrary, when

the initial state of the memory circuit is '0', the pulse causes a 2π shift of the second junction phase. Consequently, the second junction shows a corresponding voltage spike. Thus, the second junction response depends on the initial state of the circuit. However, as it is for destructive read operations, after the Read command is performed the circuit state will always be settling in state '1'. Figure 16 shows the responses of the second junction to the pulse sent to the first junction (the same as a Write "1" operation, Figures 5 and 8).

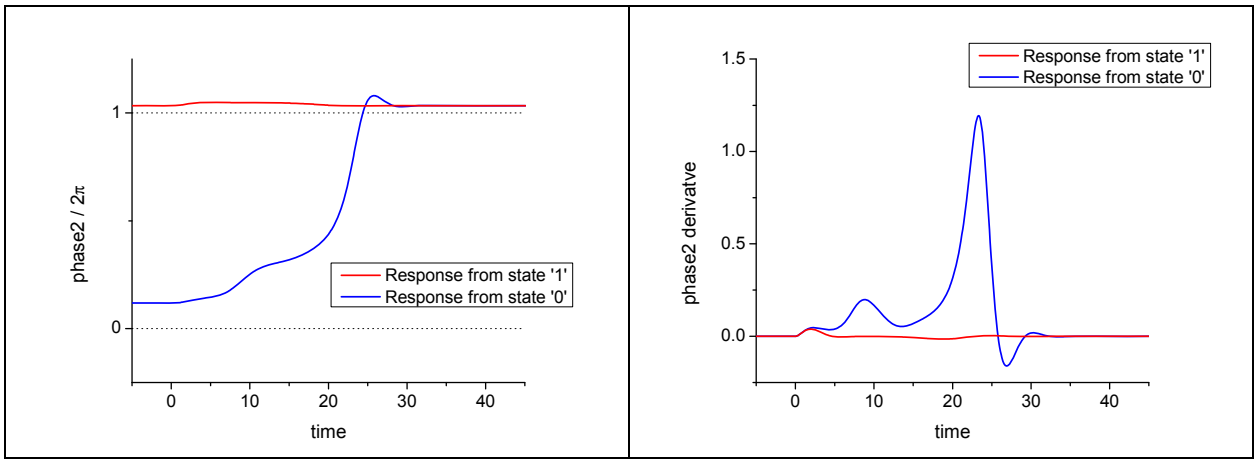

Figure 16: The time series of the second junction phase scaled by 2π (left) and second junction phase derivative, or voltage, (right) in response to a Gaussian pulse applied to the first junction when the system is in state '1' (red curves) and '0' (blue curves). $i_{pulse,1}$ = 1.0.

Read operation can also be implemented by sending a pulse to the third junction and subsequently reading the response from that same junction. Sending a pulse to the third junction will also always set the circuit to the '0' state, similar to our previous example.

In the Table 2 below we summarize the above example of the basic memory cell operations presented in this Section.

	Write '0'	Write '1'	Read
Original state '0'	Applied junction: J_3 End state: '0'	Applied junction: J_1 End state: '1'	Applied junction: J_1 End state: '1' Read junction: J_2
Original state '1'	Applied junction: J_3 End State: '0'	Applied junction: J_1 End state: '1'	Applied junction: J_3 End state: '1' Read junction: J_2

Table 2: Logics of basic memory cell operations.

Memory Performance Evaluation

In order to evaluate and improve the Josephson junction based memory circuit performance we performed an iterative optimization algorithm. The iterative algorithm employed is called Simulated Annealing (SA), a globally convergent optimization technique. SA attempts to minimize a function in a manner similar to annealing to find a global minimum of the pre-selected cost function. Corana et al. [17] implementation of SA for continuous variables is used in the present methodology in conjunction with our coupled junction simulation module. SA explores the target function's entire surface by performing random walks in *m* parameter space, where *m* represents the number of optimization variables. A rough view of the parameter space is first obtained by moving with large step lengths. As the algorithm progresses and falls, it focuses on the most promising area within the parameter space. SA attempts to optimize the function while

moving both uphill and downhill in order to escape local minima. SA has other advantages which suggest its use for the optimization of Josephson junction parameters. Firstly, unlike many iterative optimization schemes (e.g., Newton or steepest-descent schemes), SA can produce accurate results even for poor choices of initial conditions. Moreover, SA makes no assumption that a cost function is continuous, important here because we will define our cost functions to be discontinuous, as explained below. Finally, SA can be used on cost functions of arbitrary numbers of variables. For a more details about SA and its applications, see, for example, [17-19].

We employed SA procedure for external pulse and external current parameters to numerically calculate access times and access energies. Comprehensive results for optimization procedure will be reported in a different the manuscript [20] and in this manuscript we only provide a very brief summary of the results. We kept pulse and external current parameter variation in such a way that variations in theses parameters would not affect the existence of two pre-designed memory states ([0, 0, 0] – [1, 1, 0]) and would allow transitions between these states to implement valid Read, Write, and Reset operations. Such a requirement, for obvious reason, has limited the values of the parameters that can be employed. As we iterated pulse parameters in acceptable limits to stay within the prescribed/preselected states we observed that the fluctuations in access times and access energies can vary (perhaps by the factor of 1.5 - 2, or more). An example of the minimal pulse amplitudes to implement transitions from '0' state to '1' and from "1" state to "0" (and consequently, valid Write, Read, and Reset operations) as functions of the dc current amplitudes of the junctions #1 and #3 is demonstrated in the Figure 17. Note that in the Figure 17 we are showing results for larger value of the coupling constant, namely, $\kappa = 0.5$, while for other Figures in the paper we have used the value of $\kappa = 0.1$. The reason for that is that our calculation of the access time (and consequently access energies) utilizes an approximation of separable dynamics (Equations 17-29) that is accurate in the limit of the weak coupling. However, we would also like to show that the proposed logics can be applicable for much larger value of the coupling constant (thus substantially reducing the size of the memory cell).

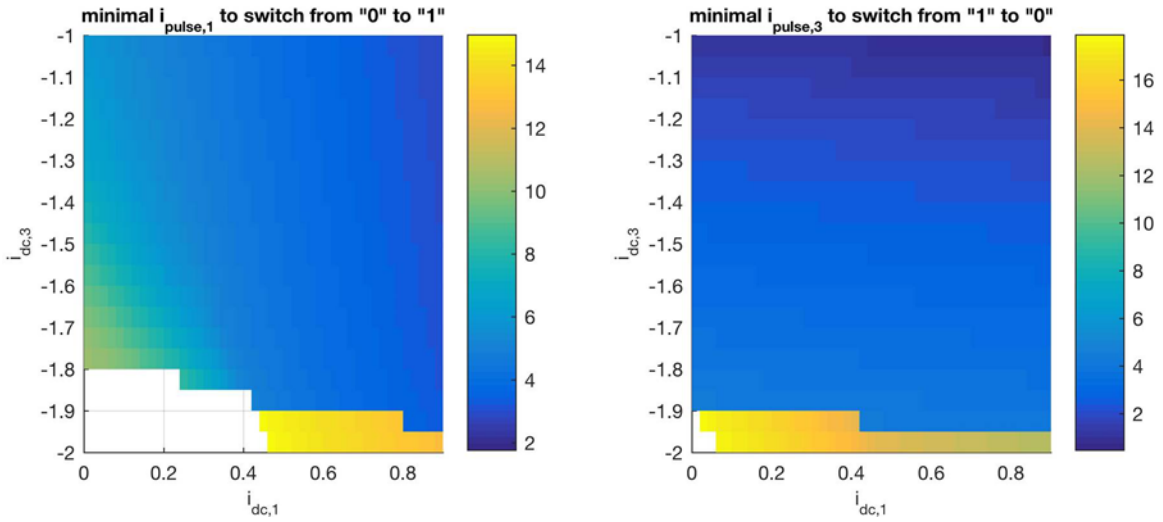

Figure 17 (Left): The minimal Gaussian pulse amplitude for transition from '0' to '1' and (Right): The minimal pulse amplitude for transition from '1' to '0' operation.

There exist some parameter range for which access times and access energies vary very modestly and for some other parameter range memory operations may be very sensitive to pulse and external current parameter values (since parameter fluctuations will alter JJ array memory states and consequently will affect memory operation). Our main conclusion is that it is indeed possible to set pulse and external current parameter values amenable for non-faulty and robust memory operation. For those parameter

values the access times are in the range of 30-100 ps (for Read, Write, and Reset operations) and access energies are in the range of 5×10^{-18} - 10^{-19} J (0.1 – 5 aJ).

We would also like to briefly discuss the scalability of the proposed memory logics to large memory cell arrays. First, we would like to note that the stability diagram of the three-junction array (see Figure 4) shows multistability consequently one can in principle design four or even possibly eight bit operation for each memory cell. It would be fascinating to explore memory states of larger arrays of coupled junctions however we would be cautious not to propose such a design (at this time) as a route for scalability to large memory cell arrays. Since in currently available memory cell array designs memory cells are operated as separate (uncoupled) components with separate access to each cell, a seemingly straightforward route towards scalability would be following currently available designs (see, for example, references 6, 21, 22, 23). Moreover, since our proposed memory cell design seems to be much less complicated and lower size than, for example, today's state-of-the-art design [6] where Read and Write operations are implemented on separate circuits, peripheral circuits such as sense and current driver circuits could be also less complex and consequently lower size and perhaps requiring lower operational energy. We would also like to note that scaling memory cell to large arrays requires consideration of all the peripheral circuits (including decoders, drivers, sense circuits, and others [6, 21-23]). Consequently, since basic current and pulse driving and pulse sensing requirement of the proposed memory cell are rather common to other memory cell designs (where scaling to 64 k-bit RAM memory arrays was demonstrated [6]) we believe that scaling to large memory arrays is likely. Moreover, proposed memory cell design and input/output requirements are simpler and lower size than other memory cell circuits (see, for example memory cell circuit in the references [6, 22]).

Summary

In this paper we demonstrated a paradigm for cryogenic memory operation and presented a specific example of a circuit that consists of three inductively coupled Josephson junctions. We have employed Josephson junction non-dimensionless parameter values that are consistent with the current state-of-the-art Josephson junction fabrication capabilities as presented in the references [13]. The principles of memory design and operation described in the paper can in principle be implemented for other Josephson junction based circuits. In the proposed circuit Write, Read, and Reset operations are implemented on the same circuit. For parameter values presented in the paper, access times are of the order of 30 - 100 ps while dissipation energy is of the order of 0.1 – 5 aJ. Wide variety of parameters can be used for memory operation in the regime of weak-to-moderate coupling ranges while so far the challenge was to increase the values of the coupling constant κ to the limit of strong coupling [20] and consequently decrease the feature size/area of the inductor. This may require modifications of the presented circuit or modifications of the single junction parameters of the circuit.

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