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Phys. Rev. B **92**, 115425 — Published 17 September 2015

DOI: [10.1103/PhysRevB.92.115425](https://doi.org/10.1103/PhysRevB.92.115425)

Single electron tunneling with “slow” insulators

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(ΩDated: August 5, 2015)

Usual paradigm in the theory of electron transport is related to the fact that the dielectric permittivity of the insulator is assumed to be constant, no time dispersion. We take into account the “slow” polarization dynamics of the dielectric layers in the tunnel barriers in the fluctuating electric fields induced by single-electron tunneling events and study transport in the single electron transistor (SET). Here “slow” dielectric implies slow compared to the characteristic time scales of the SET charging-discharging effects. We show that for strong enough polarizability, such that the induced charge on the island is comparable with the elementary charge, the transport properties of the SET substantially deviate from the known results of transport theory of SET. In particular, the Coulomb blockade is more pronounced at finite temperature, the conductance peaks change their shape and the current-voltage characteristics show the memory-effect (hysteresis). However, in contrast to SETs with ferroelectric tunnel junctions, here the periodicity of the conductance in the gate voltage is not broken, instead the period strongly depends on the polarizability of the gate-dielectric. We uncover the fine structure of the hysteresis-effect where the “large” hysteresis loop may include a number of “smaller” loops. Also we predict the memory effect in the current-voltage characteristics $I(V)$, with $I(V) \neq -I(-V)$.

PACS numbers: 77.80.-e, 72.80.Tm, 77.84.Lf

I. INTRODUCTION

The single electron transistor (SET) is one of the most studied nanosystem.^{1–7} This is possibly the simplest device where strong electron correlations and quantum nature of electron can be directly observed. It consists of two electrodes known as the drain and the source, connected through tunnel junctions to one common electrode with a low self-capacitance, known as the island. The electrical potential of the island can be tuned by a third electrode, known as the gate, capacitively coupled to the island, see Fig. 1 for equivalent circuit.

For decades there was nearly a paradigm in the theory of electron transport at nanoscale that calculating *dc*-current the permittivity of dielectric layers in tunnel nanojunctions may be taken constant, without any frequency dispersion.^{4,5,8–10} However, this paradigm is not always true. A number of physical processes contribute to the polarization of a dielectric. Some of them are fast and some are slow compared to the time scales of electric field change in the nanojunctions.^{11–20} There is a progress in the development of dielectric materials with strong and at the same time quite slow response to the external electric field.^{19,21,22} The SET is a perfect laboratory device where this physics can be studied: charging-discharging effects in the SET are controllable and have the well-defined time scales.

The Coulomb blockade suppresses electron transport except for values of the gate voltage where electrons sequentially tunnel one by one through SET from source to

drain. Electric fields in the tunnel junctions are changing in time while electrons tunnel through the island. Dielectric layers in the tunnel junctions are polarized at finite electric field. The usual assumption in the theory of SET that the polarization of any dielectric layer in the tunnel barrier instantly follows the electric field in time: $\mathbf{P}(t) = \hat{\chi} \mathbf{E}(t)$, where the constant $\hat{\chi}$ is the dielectric permittivity (tensor) of the dielectric layer.^{4,10} It follows from the last expression that the capacitance C of any tunnel junction in the SET is related to the geometric capacitance $C^{(0)}$ as $C = \epsilon C^{(0)}$, where for a flat capacitor with isotropic dielectric, $\epsilon = (1 + 4\pi\chi)$.²³ And this is the only place where the polarization appears in the “classical” theory of SET. However, these relations have limited applicability. In general, the polarization of the dielectric is nonlocal in time: $\mathbf{P}(t) = \int_{-\infty}^t \hat{\chi}(t - \tau) \mathbf{E}(\tau) d\tau$, where $\hat{\chi}(t)$ is the dynamical electric permittivity. [Here we assume the linear response regime.] The time dependence of $\hat{\chi}(t)$ implies that tuning of dielectric polarization $\mathbf{P}(t)$ by an electric field can not be done arbitrary fast. This is happening, for example in dielectric materials with polarization being due to shift of heavy and inert ions.^{12,18,20}

The response of polarization $\mathbf{P}(t)$ to the external field is characterised by the time-scale τ_P , the decay time of $\hat{\chi}(t)$. The second characteristic time-scale in the problem: the time of the electric field correlation, τ_E . For $\tau_P \ll \tau_E$ the polarization has the form $\mathbf{P}(t) \approx \hat{\chi}_0 \mathbf{E}(t)$, where $\hat{\chi}_0 = \int_{-\infty}^{\infty} \hat{\chi}(\tau) d\tau$. In the opposite case, $\tau_E \ll \tau_P$, the polarization $\mathbf{P}(t)$ does not follow the electric field

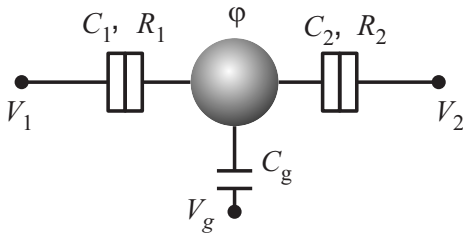


FIG. 1. (Color online) The equivalent scheme of single electron transistor (SET).⁴

$\mathcal{E}(t)$ instantaneously and it has the form

$$\mathbf{P}(t) \approx \hat{\chi} \langle \mathcal{E} \rangle, \quad (1)$$

where $\langle \mathcal{E} \rangle$ is the electric field averaged over the time scale τ_P . It follows from Eq. (1) that the simple relation for capacitance, $C = \epsilon C^{(0)}$, is not valid. Therefore the theory of single-electron tunneling in the SET should be modified and this is the main goal of our paper.

The characteristic time of charge relaxation in the SET is $\tau_\epsilon = R_\Sigma C_\Sigma$, where R_Σ is of the order of the bare tunnel resistance of the left and right tunnel junctions and C_Σ is the sum of all the capacitances, see Fig. 1. The time scale τ_ϵ is in the range of dozens of nano- to picoseconds depending on the system geometry and materials. The switching time of a dielectric material, τ_P , is in the range of seconds to femto-seconds depending on the material and the particular physical process standing behind the polarization phenomena.^{18,20}

Therefore the regime of “slow” insulator, $\tau_\epsilon \ll \tau_P$, is very important for SET-devices. However, there is paradigm that the existing theories with $\tau_P \ll \tau_\epsilon$ satisfactorily explain most experiments with SETs. What is the justification for new theory? The answer is simple: the effects discussed in this paper are especially pronounced in SETs when on average the polarization of a dielectric tunnel junction in the SET is strong enough meaning that the charge induced on the grain by the polarized dielectric is of the order of the electron charge. This condition can be reached for large enough dielectric permittivity ϵ only. How large we will discuss below.

Recently we have found a number of transport effects in the SET with slow ferroelectric in the capacitors, see Refs. 6 and 7. In particular, we investigated the memory effect in this SET. Here we uncover new physical phenomena and report about the memory-effect (hysteresis) where conductance periodicity in the gate voltage is not broken. Instead, the period strongly depends on the polarizability of the gate-dielectric due to the linear dependence of the polarization on the external field in the dielectric. Also, we uncover the unusual fine structure of the hysteresis-effect, where “large” hysteresis loop may include a number of “smaller” loops. We predict that the memory effect exists in the current-voltage characteristics, meaning that $I(V) \neq -I(-V)$ for a given hysteresis branch even at $V_g = 0$. The last two effects may exist in the ferroelectric SET, however non of them have

been found before. These results are important: SET device with hysteresis may be promising for the “shuttle” of charge^{24–26} free from moving nanomechanical degrees of freedom: cycling the gate voltage along the hysteresis loop might allow transfer of several charge quanta through the SET. Other promising applications include transistor⁴ and memory-cell. For example, the memory effect in $I(V)$ and $G(V_g)$ might help writing and reading data in(from) the polarization state.

The paper is organized as follows. In Sec. II we discuss the general properties of SET with slow dielectric and the methods for investigation of transport properties. In Sec. III we investigate the SET with slow dielectric located in the gate electrode at zero bias voltage, $V_2 - V_1$. In Sec. IV we consider the case with slow dielectric in the left and right tunnel barriers of the SET and uncover the memory effect in the current-voltage characteristics, $I(V)$. Finally, in Sec. V we discuss the validity of our approach and the requirements for slow dielectric materials which are necessary to observe the effects predicted in this paper. In the same section we show that the Coulomb blockade in SET with slow dielectrics is less affected by temperature.

II. ELECTRON TRANSPORT THROUGH SET WITH SLOW TUNNEL BARRIERS

A. Model

Consider the single electron transistor depicted in Fig. 1. Two side electrodes serve as the transistor source and drain. Electric current flows through the transistor channel which is the metal island placed in between leads and connected to the source and drain by the tunnel junctions. Bottom gate electrode controls electron transport through the channel. Current does not flow through the gate electrode (similar to the field effect transistors). Theory of “classical” SET is developed in Refs. 2–5. Essential feature of the SET discussed here is related to the fact that the gate capacitor or (and) tunnel junction capacitors are filled with a dielectric material with some special properties. This dielectric material has a very long response time, leading to essential time dispersion of the capacitor. As a result the electric polarization of the gate capacitor should be considered in a special way.

In the following it is convenient to distinguish between the geometrical junction capacitances $C_i^{(0)}$ and the low-frequency capacitances C_i that include the slow dielectric response. The difference between them, aside from the unimportant geometrical factor, is

$$\Delta C_i = C_i - C_i^{(0)} = \alpha_i S_i / d_i, \quad (2)$$

where α_i is the dielectric polarizability of the i -th junction ($i = 1, 2, g$), S_i is the junction surface area and d_i is the effective electrode-island distance. So defined α_i includes all the demagnetization factors related to the

geometry of the capacitors and effects related to nonuniform and anisotropic dielectric layers.²³ For a flat capacitor with isotropic dielectric, $C^{(0)} = S/4\pi d$ and $\alpha = \chi$.

We assume that the electrodes are biased with the voltages $V_1 = -V/2$, $V_2 = V/2$ and V_g . The grain potential $\phi(n)$ at a given number of excess electrons n can be found balancing the induced charges:

$$ne = \sum_i C_i^{(0)}(\phi(n) - V_i) + \sum_i \Delta C_i(\langle\phi\rangle - V_i), \quad (3)$$

$$\langle\phi\rangle = \sum_{n'=-\infty}^{\infty} p_{n'}\phi(n'), \quad (4)$$

where p_n is the probability to find n excess charges on the grain. Two terms originate in (3) because we distinguish the electric field produced by the capacitance $C_i^{(0)}$ and the contribution due to polarized dielectric with slow response. So the terms proportional to the coefficient ΔC_i in Eq. (4) can be considered as charges induced on the grain by the polarized dielectric layers that are constant in tunneling events.

The probability distribution p_n in the steady state can be found using the detailed balance equation²⁻⁵

$$p_n \Gamma^{n \rightarrow n+1} = p_{n+1} \Gamma^{n+1 \rightarrow n}, \quad (5)$$

where the rate $\Gamma^{n \rightarrow n+1}[V_i, n, \langle\phi\rangle]$ describes the change of grain charge from n to $n+1$ electrons. The electric current has the form

$$I = e \sum_{n=-\infty}^{\infty} p_n [\Gamma_s^{n \rightarrow n-1} - \Gamma_s^{n \rightarrow n+1}]. \quad (6)$$

Here the lower index of Γ refers to the tunneling rate corresponding to the particular tunnel junction, $s = 1$ or 2 and the rate Γ in Eq. (5) is equal to $\Gamma_1 + \Gamma_2$. Solving Eqs. (3)-(5) self-consistently we find the current-voltage characteristics of the SET using Eq. (6).

We use the “orthodox” theory²⁻⁵ to calculate the Coulomb-blockade peaks in the differential conductance of the SET. It implies that the tunnel junction resistances $R_{1,2}$ are much larger than the resistance quantum $R_q = h/e^2$: this condition insures perfect quantization of the excess charge on the island. The temperature T must be much smaller than the charging energy (it is of the order of electrostatic energy of one excess electron on the island), see Sec. V D for discussion about the correct definition of the charging energy. Also electron level spacing on the island should be smaller than temperature, see Sec. V.

In the leading order the probability per unit time to change the island occupation number from n to $n \pm 1$ through the first junction is given by the Fermi golden rule

$$\Gamma_{n \rightarrow n \pm 1}^{(1)} = \frac{1}{e^2 R_1} \cdot \Delta F_1^{n \rightarrow n \pm 1} N_B(\Delta F_1^{n \rightarrow n \pm 1}), \quad (7)$$

where $N_B(\omega) = 1/[\exp(\omega/T) - 1]$ is the Bose-function,^{4,27} R_1 is the tunnel junction resistance and $\Delta F_1^{n \rightarrow n \pm 1}$ denotes the free energy change with Q'_0 being the effective charge

$$\Delta F_1^{n \rightarrow n \pm 1} = \Delta U_n^\pm \mp W_1, \quad (8)$$

where $\mp W_1$ is the work done by the leads and the gate to transfer an electron to/from the grain through the first tunnel junction. The calculation of Γ -rates requires the knowledge of the difference in the electrostatic energies when the number of excess charges on the grain differ by one elementary charge: $\Delta U_n^\pm = U(n \pm 1) - U(n)$. If the polarization in dielectric layers on electron jumps follow ϕ adiabatically, $P_i = \alpha_i(\phi - V_i)/d_i$, we have $\Delta U_n^\pm = E_c(1 \pm 2n)$, where $E_c = e^2/2C_\Sigma$ with all the capacitances $C_\Sigma = \sum_i C_i$ being properly renormalized, $C_i = C_i^{(0)}(1 + 4\pi\alpha_i)$. However, for slow dielectric layers the polarization $P_i = \alpha_i(\langle\phi\rangle - V_i)/d_i$ stays constant during the tunneling, and for the energy difference we find (see App. A)

$$\Delta U_n^\pm = E_c^{(0)}(1 \pm 2n \mp 2 \sum_i P_i S_i / e), \quad (9)$$

where $E_c^{(0)} = e^2/2C_\Sigma^{(0)}$, $C_\Sigma^{(0)} = \sum_i C_i^{(0)}$ and $P_i S_i = \Delta C_i(\langle\phi\rangle - V_i)$.

The work done by the leads and the gate to transfer an electron to/from the grain remains the same as in the “orthodox” theory²⁻⁵ except for the fact that only the geometrical capacitances $C_i^{(0)}$ should be taken into account:

$$W_1 = \frac{e([C_g^{(0)} + C_2^{(0)}]V_1 - C_2^{(0)}V_2 + Q')}{C_\Sigma^{(0)}}, \quad (10)$$

$$W_2 = \frac{e([C_g^{(0)} + C_1^{(0)}]V_2 - C_1^{(0)}V_1 + Q')}{C_\Sigma^{(0)}}, \quad (11)$$

where the effective gate-induced charge Q' is

$$Q' = -C_g^{(0)}V_g + \sum_i \Delta C_i(\langle\phi\rangle - V_i). \quad (12)$$

This in particular implies that for temperature $T \rightarrow 0$ the effective ground state free energy is defined as

$$F_0 = E_c^{(0)} \min(n - Q'/e)^2, \quad (13)$$

Below we use the notation $Q = -C_g V_g$ for the traditional gate-induced charge. We show that although the effects of slow polarization are far from being a simple renormalization of capacitances $C_i^{(0)} \rightarrow C_i$, the conductance periodicity in Q holds and maintains its period $|e|$ for any values of the parameters ΔC_i .

B. Nature of the memory effect: analytical estimates

The detailed balance equation (5) can be solved analytically for the set of voltages V_g near the “degeneracy points”, where the ground state energy of the SET

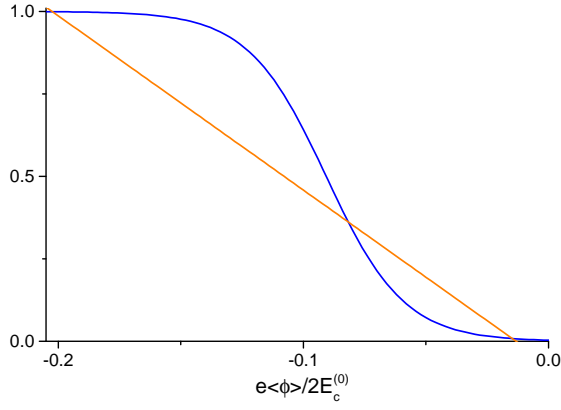


FIG. 2. (Color online) Graphical solution of Eq. (14) showing three possible solutions for an average grain potential $\langle\phi\rangle$ at a given gate voltage V_g . Parameters are: $Q = -0.07|e|$, $C_g^{(0)} = 0.5C_\Sigma^{(0)}$, $\Delta C_g/C_\Sigma^{(0)} = 0.5$, and $T = 0.4E_c^{(0)}$. The three distinct solutions for $\langle\phi\rangle$ at a given Q_0 correspond to the memory effect instability.

changes from n to $n \pm 1$ excess charges. The last condition requires the effective charge Q' to be close to $e(n + 1/2)$. In this case the only two probabilities p_n are finite while the other probabilities are exponentially suppressed by the factor $e^{-E_c^{(0)}/T}$. In order to illustrate the origin of the memory effect, we will focus on the degeneracy point between $n = 0$ and $n = 1$ at $V_{1,2} = 0$. Using Eqs. (3)-(4) we find for the average potential $\langle\phi\rangle$

$$n_F[(1 - 2Q'/e)E_c^{(0)}] = e\langle\phi\rangle/2E_c^{(0)} + Q'/e, \quad (14)$$

where n_F is the Fermi-function. Equation (14) has one or three solutions for a given gate voltage Q . The latter case is shown in Fig. 2. The presence of three distinct solutions for the average potential $\langle\phi\rangle$ at a given parameter Q indicates the memory effect instability. Using the graphical solution of Eq. (14) we estimate the criteria for the memory effect instability, $\sum_i \Delta C_i/C_\Sigma^{(0)} \gtrsim 2T/E_c^{(0)}$. This criterion corresponds to the critical value of ΔC_Σ when the memory effect just appears, see Eq. (36) below for the exact expression.

III. SET WITH SLOW INSULATOR IN THE GATE CAPACITOR

A. Numerical study of electron transport through SET

Here we study electron transport through SET numerically. We consider the SET with slow dielectric layer in the gate capacitor. This set-up is the most favourable for experiment since in this case there is no electron tunneling through the gate electrode and it can be arbitrary thick to allow a wide choice of dielectric materials. Moreover, as we will show in the following Sec. IV, at $V = 0$

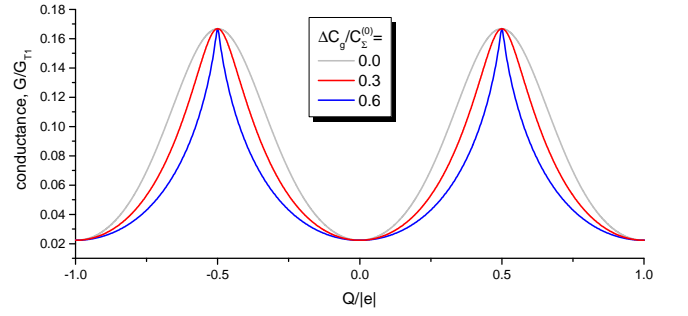


FIG. 3. (Color online) Conductance peaks for $\Delta C_g/C_\Sigma^{(0)} = 0, 0.3, 0.6$. The “unit” of conductance G_{T1} is the conductance of the first tunnel junction of the SET. Parameters are: capacitances $C_1^{(0)} = 0.3C_\Sigma^{(0)}$, $C_2^{(0)} = 0.5C_\Sigma^{(0)}$ and $C_g^{(0)} = 0.2C_\Sigma^{(0)}$ and temperature $T = 0.2E_c^{(0)}$. The slow dielectric in the gate capacitor modifies the shape of the conductance peaks but preserves the periodicity in parameter Q in contrast to the SET with ferroelectric in the gate capacitor.⁷

by considering the gate capacitor we still preserve all the qualitative effects introduced by slow dielectrics in a general case.

Thus, for a time, we assume that the only non-zero ΔC is ΔC_g .

For $\Delta C_g = 0$ the conductance is a periodic function of the effective gate voltage Q , see the gray curve in Fig. 3. The conductance peaks are well fitted by the orthodox theory where near the peak maximum the conductance is

$$G^{(0)}(\delta Q^{(0)}) \approx \frac{e \delta Q^{(0)}/C_\Sigma^{(0)} T}{2(R_1 + R_2) \sinh(e \delta Q^{(0)}/C_\Sigma^{(0)} T)}. \quad (15)$$

Here $\delta Q^{(0)}/e = \min_k [-C_g^{(0)} V_g/e - (2k + 1)/2] \ll 1$.

At finite but small ΔC_g , when the induced charge on the island due to polarization is smaller than the elementary charge, the conductance peaks change their shape, but preserve their amplitude and position (see Fig. 3).

The opposite case, with dielectric polarization being strong enough to induce the charge on the island of the order of the elementary charge or larger, is more interesting. In this case the conductance peaks show the hysteresis and their shape depends on the direction of Q -evolution, see Fig. 4. The hysteresis appears for $\Delta C_g \gtrsim C_\Sigma^{(0)} 2T/E_c^{(0)}$ (see Eq. 29). Despite the memory effect the conductance remains periodic in the renormalized gate voltage $Q = -(C_g^{(0)} + \Delta C_g)V_g$ with the same period $|e|$ for any ΔC_g . This behavior is in striking contrast to the SET with ferroelectric in the gate where due to the nonlinearity of polarization–electric field dependence the periodicity of conductance is broken, see Ref. 7.

Now we discuss the structure of the memory effect. Above the critical value of ΔC_g there are many brunch-solutions of the self-consistency equation for the average grain potential, Eq. (4), for the given temperature, bias

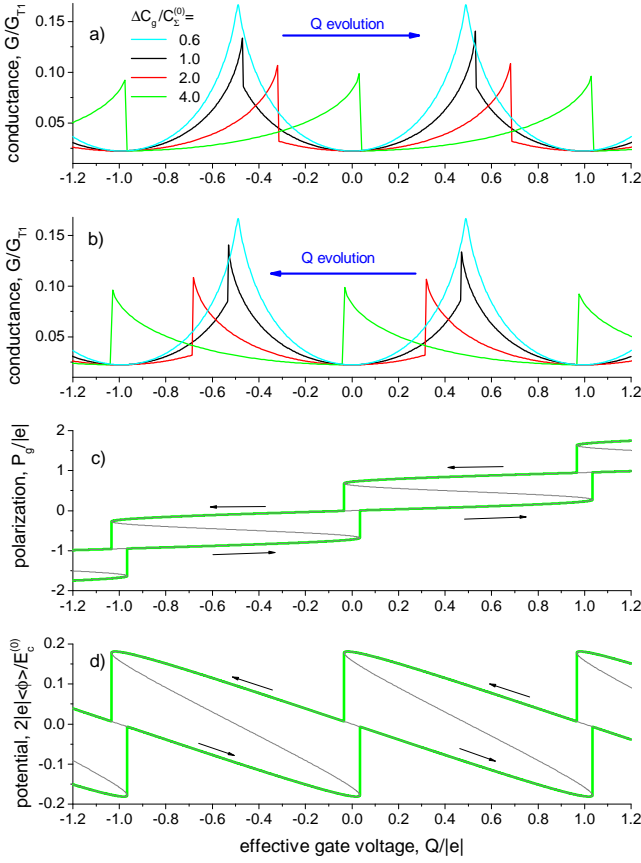


FIG. 4. (Color online) Memory effect instability in the SET with slow insulator in the gate capacitor. (a) and (b) the conductance branches corresponding to the increasing and decreasing parameter Q and $\Delta C_g/C_\Sigma^{(0)} = 0.6, 1, 2, 4$, (c) polarization and (d) the average grain potential (arrows show the direction of Q evolution for a given branch) for $\Delta C_g/C_\Sigma^{(0)} = 4$. Grey lines show stable and unstable branches of polarization and the average potential. Parameters are: capacitances $C_1^{(0)} = 0.3C_\Sigma^{(0)}$, $C_2^{(0)} = 0.5C_\Sigma^{(0)}$ and $C_g^{(0)} = 0.2C_\Sigma^{(0)}$ and temperature $T = 0.2E_c^{(0)}$ as in Fig. 3.

and gate voltage. The question is - how to choose the right branch? Figure 5 provides an answer to this question. According to the branching theory²⁸ the jumps occur at the “branching points” where the observable has an infinite derivative in parameter Q . On the other hand, the branch should correspond to the minimum of some effective energy functional. In our case (no bias) the role of the effective energy plays the free energy

$$F = -T \ln Z, \quad Z = \sum_n \exp \left(-\frac{E_c^{(0)} (n - Q'/e)^2}{T} \right). \quad (16)$$

For zero temperature it reduces to the free energy F_0 discussed above.

The plots of the free energy have a similar dependence on the parameter Q as the zero-bias conductance G . To illustrate this point we show in Fig. 6 the free energy for

$\Delta C_g/C_\Sigma^{(0)} = 0.6, 1.3$. Figure 5b shows that the conductance branch between points “A” and “B” is metastable: the free energy for this curve is larger than the free energy for branch below. However, during the adiabatically slow increase of parameter Q the system does not switch to the lowest branch at point A, instead it may go up to the metastable branch. The same applies to all other plots in Fig. 6. The external perturbation can drive the system to outside of the metastable branch before the bifurcation point. Usually the role of this “perturbation” plays the Langevin forces induced by the thermostat. In this case the jumps occur randomly within the same region before the bifurcation point. This scenario is typical for any hysteresis.

Intuitively one may suppose that if conductance “jumps” from one branch to another the final branch should have the lowest possible free energy for the parameter Q corresponding to the jump. Indeed, this is the case in Figs. 5(a)-(c). However, in Figs. 5(d) and (f) this rule is violated. The system could jump, for example, to the point marked by the red-ball in Fig. 5(d), instead of finishing at the point marked by the grey-ball which has a larger free energy. However, this energetically favourable transition is “forbidden”: while continuously changing the polarization in such a process the system would have to pass the energy barrier of approximately $E_c^{(0)}/4$ (free energy maximum). Thus the higher order jumps (over the average charge difference) are suppressed by the factor $\exp(-E_c^{(0)}/4T)$.

B. The fine structure of the memory effect

Doing numerical studies of memory effect we assumed that parameter Q increases (or decreases) monotonically from minus to plus infinity (or vice-versa). However, for large enough parameter ΔC_g , when polarization induces more than one electron on the grain, the hysteresis loop depends on the interval where the parameter Q changes. This is shown in Fig. 7 with two possible hysteresis loops: The red hysteresis loop corresponds to back and forth change of parameter Q in the interval $(-2, 1)$ while the blue curve corresponds to the interval $(-2, 2)$. In the second case the larger hysteresis loop “includes” smaller loops. As a result, the understanding of memory effect at finite intervals of parameter Q evolution requires consideration of all branches of the SET observables such as conductance and polarization.

C. Analytical description of the conductance peaks and the memory effect

Here we present the analytical description of transport properties of SET. At $V = 0$ and within the two-state approximation the form of the conductance peaks $G(Q)$ can be found using Eq. (15) with the proper substitution $Q^{(0)} \rightarrow Q'$, where Q' is defined in Eq. (12): with this

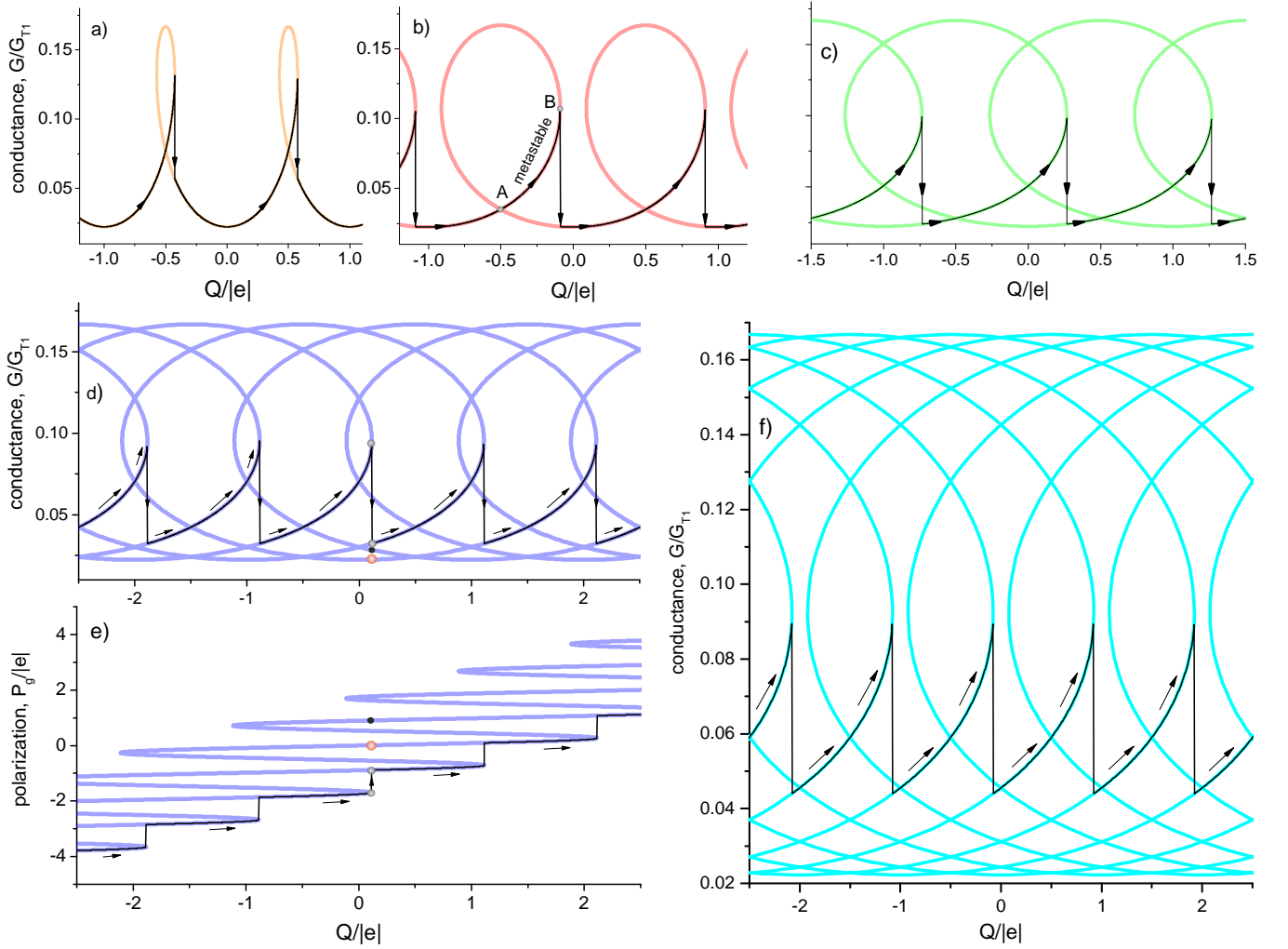


FIG. 5. (Color online) Memory effect: Plots (a)-(d) and (f) show the conductance for $\Delta C_g / C_{\Sigma}^{(0)} = 1.3, 3.3, 5.3, 10, 20$ for stable and unstable branches of Eq.(4) for the average grain potential. Plot (e) shows the polarization for $\Delta C_g / C_{\Sigma}^{(0)} = 10$. Arrows indicate the position of hysteresis jumps for particular branch with increasing Q . All plots are shown at fixed temperature $T = 0.2E_c^{(0)}$.

substitution we have for conductance $G(Q) = G^{(0)}(Q')$. For average potential, generalizing Eq. (14), we obtain

$$\langle \phi \rangle = \frac{e}{C_{\Sigma}^{(0)}} \left(\frac{1}{2} \tanh \left(\frac{E_c^{(0)}}{T} \frac{\delta Q'}{e} \right) - \frac{\delta Q'}{e} \right), \quad (17)$$

where $\delta Q'/e = \min_k(Q'/e - (k + 1/2))$. Combining Eqs. (17) with (12) we find,

$$\delta Q' \frac{C_{\Sigma}}{C_{\Sigma}^{(0)}} - \frac{e}{2} \frac{\Delta C_g}{C_{\Sigma}^{(0)}} \tanh \left(\frac{E_c^{(0)}}{T} \frac{\delta Q'}{e} \right) = \delta Q, \quad (18)$$

where $\delta Q = Q - (k + 1/2)e$ is the deviation of parameter Q , k is the same as for $\delta Q'$ and $C_{\Sigma} = C_{\Sigma}^{(0)} + \Delta C_g$. It should be noted that the above equations are valid for any δQ as long as $\delta Q' \ll 1$.

1. Small polarization

Here we discuss the limit of small polarization, meaning that the induced charge on the island is small compared to the elementary charge e . Using the small parameter, $\Delta C_g / C_{\Sigma}^{(0)} \ll 1$, we expand Eq. (18) up to the second order

$$(\delta Q')_0 = \delta Q \frac{C_{\Sigma}^{(0)}}{C_{\Sigma}}, \quad (19)$$

$$(\delta Q')_1 = (\delta Q')_0 + \frac{e}{2} \frac{\Delta C_g}{C_{\Sigma}} \tanh \left(\frac{E_c^{(0)}}{T} \frac{(\delta Q')_0}{e} \right). \quad (20)$$

The conductance now may be found by substituting $\delta Q^{(0)}$ with $(\delta Q')_{0,1}$ in Eq. 15.

$$G(\delta Q) = G^{(0)}(\delta Q') \quad (21)$$

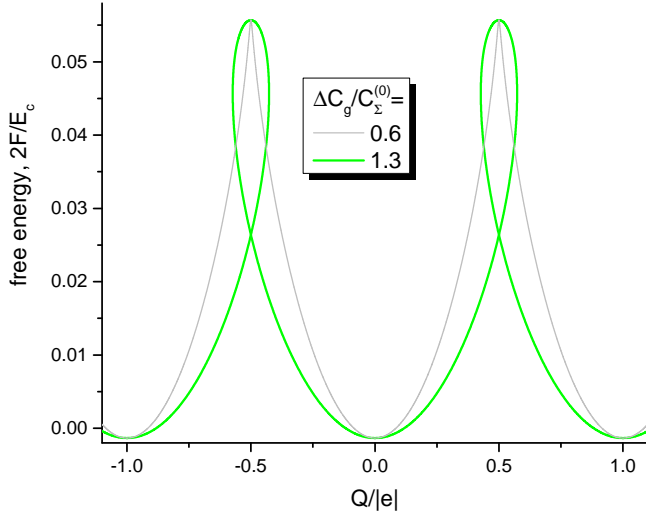


FIG. 6. (Color online) Free energy in Eq.(16) for $\Delta C_g/C_\Sigma^{(0)} = 0.6, 1.3$ and temperature $T = 0.2E_c^{(0)}$. The shape of free energy plot is similar to the conductance $G(Q)$ plot in Fig. 5a.

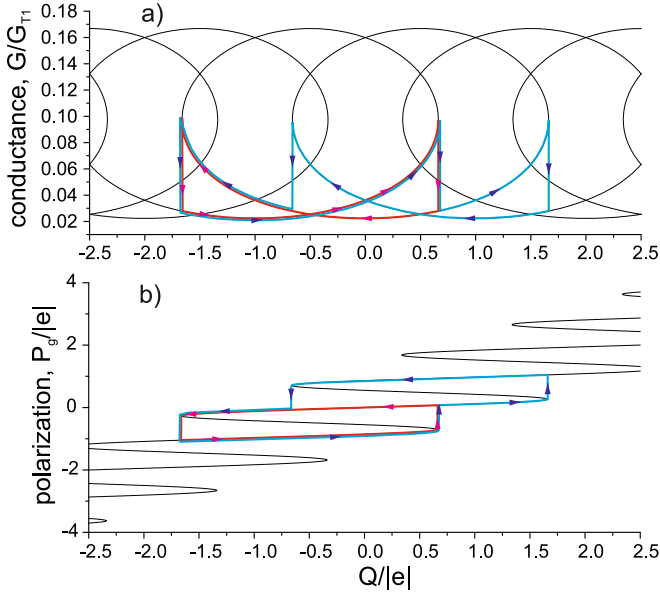


FIG. 7. (Color online) Memory effect in (a) the conductance and (b) the polarization of the gate-insulator. The red hysteresis loop corresponds to back and forth change of parameter Q in the interval $(-2, 1)$, while the blue curve corresponds to $(-2, 2)$ interval. Parameters are: $\Delta C_g = 7.5C_\Sigma^{(0)}$, $T = 0.2E_c^{(0)}$, while $C_i^{(0)}$, $i = 1, 2, g$ and R_j , $j = 1, 2$ similar to Fig. 3.

The numerical calculations in Fig. 8(a) show that the first order approximation, Eq. (20), well describes the peak shape for small parameter $\Delta C_g/C_\Sigma^{(0)} \approx 0.1$, while the zero order approximation is not sufficient. We note that parameter $\Delta C_g/C_\Sigma^{(0)}$ and thus the renormalization of the conductance period over V_g can be arbitrary in this approximation.

2. Amplitude and form of the conductance peak in the hysteresis regime

Solution of Eq. (18) becomes ambiguous for large values of parameter ΔC_g , where conductance $G(Q)$ acquires hysteresis. In this case the form of conductance peaks becomes nonsymmetric and the conductance $G(Q)$ has a maximum at the branching (bifurcation) point corresponding to the jump of the polarization. The bifurcation points in Eq. (18) can be found as follows

$$\frac{d}{dQ'} \left(\delta Q' \frac{C_\Sigma}{C_\Sigma^{(0)}} - \frac{e}{2} \frac{\Delta C_g}{C_\Sigma^{(0)}} \tanh \left(\frac{E_c^{(0)}}{T} \frac{\delta Q'}{e} \right) \right) = 0, \quad (22)$$

that reduces to

$$\cosh^2 \left(\frac{E_c^{(0)}}{T} \frac{(\delta Q')_{\max}}{e} \right) = \frac{E_c^{(0)}}{2T} \frac{\Delta C_g}{C_\Sigma}. \quad (23)$$

The two solutions of Eq. (23) correspond to the increasing and decreasing evolution of parameter Q (solutions with $\delta Q' < 0$ and $\delta Q' > 0$ respectively). These two solutions result in mirror-reflected shapes for the peaks, so we focus only on the decreasing parameter Q . For conductance maximum we find

$$G_{\max} = \frac{1}{2(R_1 + R_2)} \frac{\operatorname{arccosh} \left(\sqrt{\frac{E_c^{(0)}}{2T} \frac{\Delta C_g}{C_\Sigma}} \right)}{\sqrt{\frac{E_c^{(0)}}{2T} \frac{\Delta C_g}{C_\Sigma} \left(\frac{E_c^{(0)}}{2T} \frac{\Delta C_g}{C_\Sigma} - 1 \right)}}. \quad (24)$$

The predicted conductance maximum amplitude variation is shown in Fig. 8. One can see that the curve breaks at critical value of parameter ΔC_g indicating the start of the hysteresis regime.

We note that since within the scope of the two-state approximation and for ΔC_g above the critical value the Eq. (24) gives exact maximum, its applicability depends only on temperature. At finite ΔC_g the conductance maximum does not exactly correspond to a degeneracy point $\delta Q' = 0$, but still $\delta(Q')_{\max} \ll 1$ for $T \ll E_c^{(0)}$. For example, for temperature $T = 0.06E_c^{(0)}$ and $\Delta C_g \rightarrow \infty$ we have $\delta(Q')_{\max}/|e| \approx 0.1 \ll 1$, meaning that our consideration is valid (see Fig. 8).

Now we find the form of conductance peaks. Expanding Eq. (18) up to the second order near $\delta(Q')_{\max}$ we obtain

$$A_0 + A_2(\delta Q' - \delta(Q')_{\max})^2 = \delta Q, \quad (25)$$

where

$$A_0 = \frac{eT}{E_c^{(0)}} \frac{C_\Sigma}{C_\Sigma^{(0)}} \operatorname{arccosh} \left(\sqrt{\frac{E_c}{2T} \frac{\Delta C_g}{C_\Sigma}} \right) - \frac{e}{2} \frac{\Delta C_g}{C_\Sigma^{(0)}} \sqrt{1 - \frac{2T}{E_c^{(0)}} \frac{C_\Sigma}{\Delta C_g}}, \quad (26)$$

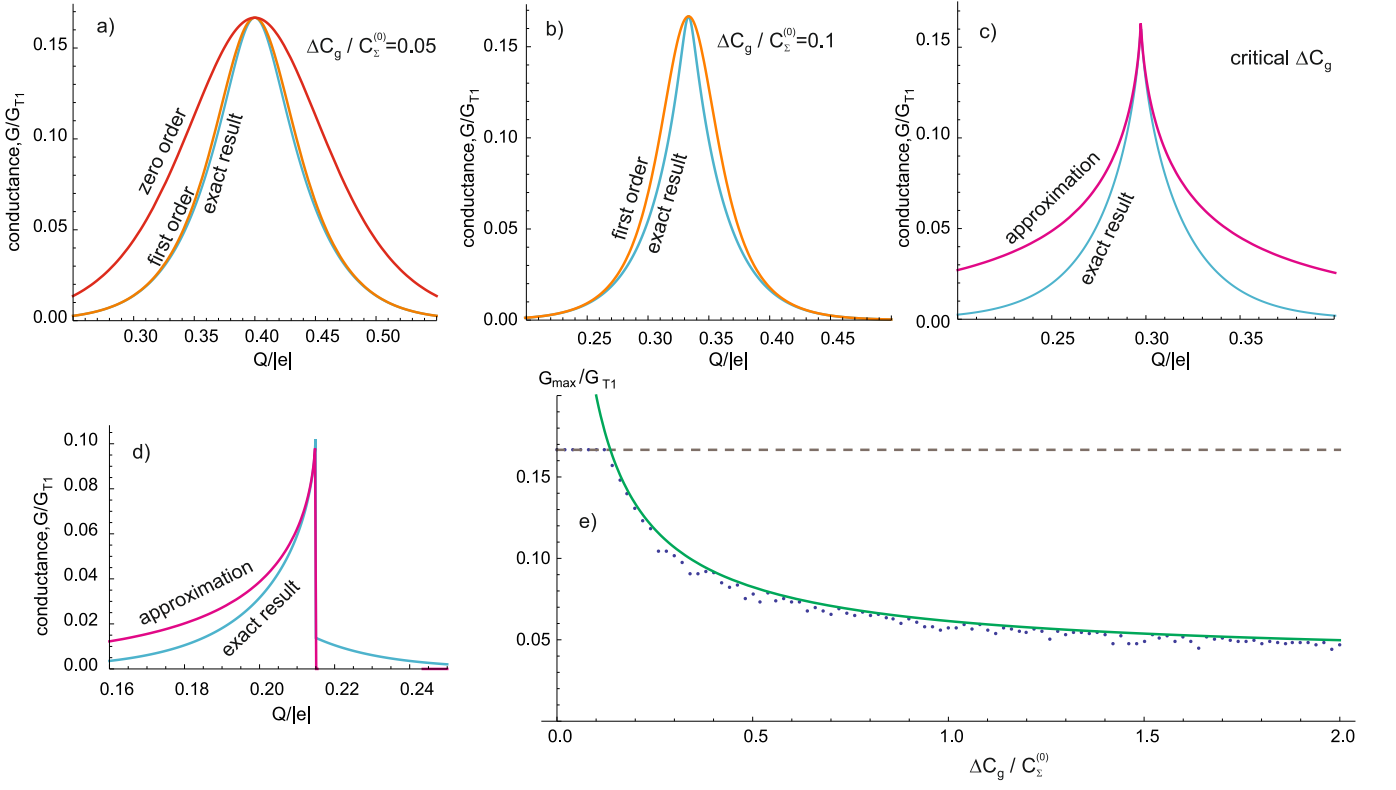


FIG. 8. (Color online) (a) Numerical solution for conductance peak for $\Delta C_g / C_\Sigma^{(0)} = 0.05$ (blue line), orange line is the zero order solution from Eq. (19), and the red line is the first order solution from Eq. (20). (b) Numerical and analytical solutions of conductance for $\Delta C_g / C_\Sigma^{(0)} = 0.1$. The first order approximates well the conductance peak at small ΔC_g . (c) Conductance at critical ΔC_g , where hysteresis appears. (d) Conductance hysteresis. (e) Amplitude of conductance peak vs ΔC_g . Points represent the numerical solution; the dashed curve is $G_{\max} = 1/2(R_1 + R_2)$; and the green solid curve shows Eq. (24) for G_{\max} . Parameters are: $T = 0.06 E_c^{(0)}$, while $C_1^{(0)}$, $C_2^{(0)}$, $C_g^{(0)}$ and $R_{1,2}$ are the same as in Fig. 3.

and

$$A_2 = \frac{E_c^{(0)}}{eT} \frac{C_\Sigma}{C_\Sigma^{(0)}} \sqrt{1 - \frac{2T}{E_c^{(0)}} \frac{C_\Sigma}{\Delta C_g}}. \quad (27)$$

It follows from Eqs. (25) and (21) that the conductance derivative in δQ diverges as $1/\sqrt{x}$ near its maximum value.

3. The peak form at the bifurcation point

To find the conductance peak at the critical value of parameter ΔC_g we expand the hyperbolic tangents in Eq. (18) up to the third order. As a result we obtain

$$\delta Q' \left(1 - \frac{\Delta C_g}{C_\Sigma^{(0)}} \left(\frac{E_c^{(0)}}{2T} - 1 \right) \right) + \frac{e \Delta C_g}{6 C_\Sigma^{(0)}} \left(\frac{E_c^{(0)}}{T} \frac{\delta Q'}{e} \right)^3 = \delta Q. \quad (28)$$

The linear term equals zero at the critical point. For critical polarizability of the gate-insulator we find

$$\Delta C_g^{(c)} = C_\Sigma^{(0)} (E_c^{(0)} / 2T - 1)^{-1}. \quad (29)$$

Also we find that

$$\delta Q' = \frac{eT}{E_c^{(0)}} \sqrt[3]{6 \frac{\delta Q}{e} \left(\frac{E_c^{(0)}}{2T} - 1 \right)}. \quad (30)$$

Using Eq. (21) we find that the peak maximum can be approximated with the function $1/(1+x^{2/3})$ (here $x \propto \delta Q$), while the derivative diverges at the conductance maximum as $1/\sqrt[3]{x}$. As follows from Fig. 8(c) and Eq. (30) this approximation for conductance works well near its maximum value only.

IV. SINGLE ELECTRON TUNNELING THROUGH SLOW DIELECTRIC LAYER

A. Conductance peaks with slow dielectrics in all capacitors

Here we consider the general case, with slow dielectric layers in all capacitors with polarizabilities ΔC_1 , ΔC_2

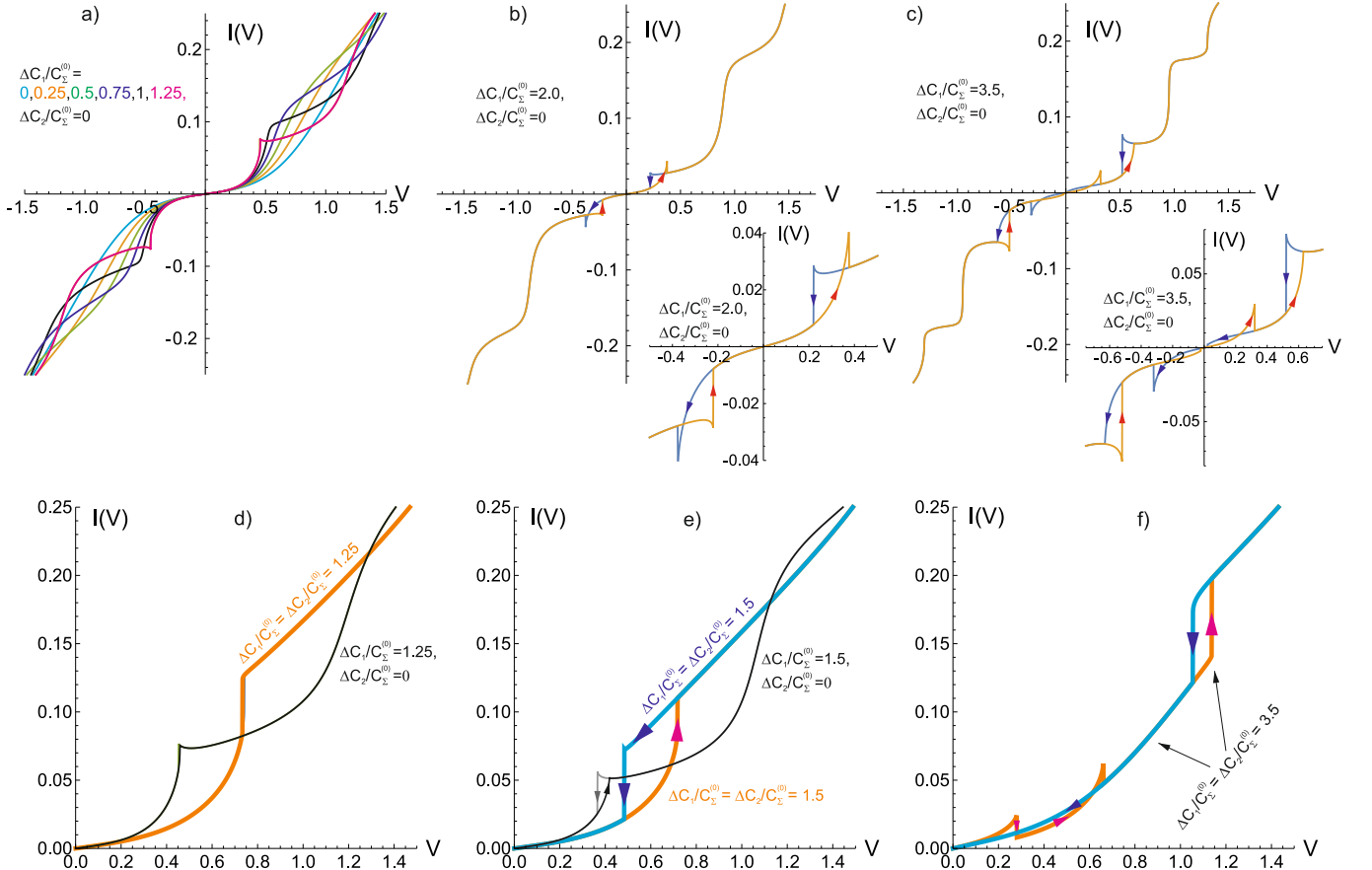


FIG. 9. (Color online) Current-voltage characteristics, $I(V)$ of SET with zero gate-capacitance, $C_g = 0$. Plot (a) shows $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = 0.0, 0.25, 0.5, 0.75, 1.0, 1.25$. Smoother curves correspond to smaller ΔC_1 . Plot (b) corresponds to $\Delta C_1/C_\Sigma^{(0)} = 1.5$. The jumps in $I(V)$ in (b), (c), and (e), (f) correspond to the memory effect: the branch depends on the direction of voltage change. Plot (c) shows $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = 3.5$. The $I(V)$ -curve can have many hysteresis loops depending on the amount of electron charge induced on the grain by the dielectric polarization. Inserts in (b), (c) show the details of the hysteresis. Plot (d) shows $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = 1.25$, $\Delta C_2/C_\Sigma^{(0)} = 0$ (black curve) and $\Delta C_1/C_\Sigma^{(0)} = \Delta C_2/C_\Sigma^{(0)} = 1.25$ (orange curve), while plot (e) shows the graphs for $\Delta C_1/C_\Sigma^{(0)} = 1.5$, $\Delta C_2/C_\Sigma^{(0)} = 0$ (black curve) and $\Delta C_1/C_\Sigma^{(0)} = \Delta C_2/C_\Sigma^{(0)} = 1.5$ (orange and blue curves). Plot (f) shows $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = \Delta C_2/C_\Sigma^{(0)} = 3.5$. Parameters are: $T = 0.06 E_c^{(0)}$, $C_1^{(0)} = 0.6 C_\Sigma^{(0)}$, $C_2^{(0)} = 0.4 C_\Sigma^{(0)}$, and R_i , $i = 1, 2$ similar to Fig. 3. The unit of voltage is $E_c^{(0)}/|e|$, and the current is normalised to $E_c^{(0)}/|e|R_{T1}$.

ΔC_g . Using Eq. (12) we find

$$Q' = Q + \Delta C_\Sigma \times \langle \phi \rangle(Q', V) - (\Delta C_2 - \Delta C_1) \frac{V}{2}, \quad (31)$$

where we introduce the parameter

$$\Delta C_\Sigma = \sum_{i=1,2,g} \Delta C_i. \quad (32)$$

Here we explicitly show that the functions Q' and $\langle \phi \rangle$ depend on voltage V . In general, this dependence results in an additional contribution to the conductance proportional to $\partial Q'/\partial V$:

$$G(Q, V) = \frac{\partial I^{(0)}(Q', V)}{\partial V} = G^{(0)}(Q', V) + \frac{\partial I^{(0)}(Q', V)}{\partial Q'} \frac{\partial Q'}{\partial V}, \quad (33)$$

where $I^{(0)}(Q, V)$ is the current in the orthodox theory, generally not limited by the two-state approximation. However, the current I is zero for zero bias voltage for any Q , therefore the last term can be omitted at $V = 0$. This explains why in two-state approximation we can calculate the conductance by replacing Q by Q' in Eq. (15) of the orthodox theory.

For zero voltage, $V = 0$, Eq. (31) reduces to

$$Q' = Q + \Delta C_\Sigma \times \langle \phi \rangle(Q'). \quad (34)$$

Then

$$\delta Q' \left(1 + \frac{\Delta C_\Sigma}{C_\Sigma^{(0)}} \right) - \frac{e}{2} \frac{\Delta C_\Sigma}{C_\Sigma^{(0)}} \tanh \left(\frac{E_c^{(0)}}{T} \frac{\delta Q'}{e} \right) = \delta Q. \quad (35)$$

As we can see, the only distinction of the Eq. 35 from Eq. 18 is the replacement of ΔC_g with ΔC_Σ . It follows

that for $V = 0$ the SET with slow insulators in tunnel junctions behaves qualitatively similar to the only $\Delta C_g > 0$ that was considered previously. The only difference is related to the fact that the slow dielectric in the gate capacitor renormalizes the period of the Q -oscillations of conductance while slow dielectrics in all other capacitors of the SET do not.

Now we can generalize our results for positive $\Delta C_g > 0$ obtained earlier. In particular, the critical polarization, where memory effect in the conductance $G(Q)$ first appears, becomes the integral quantity, see Eq. (32), that includes properties of all the slow dielectric layers:

$$\Delta C_\Sigma^{(c)} = C_\Sigma^{(0)}(E_c^{(0)}/2T - 1)^{-1}. \quad (36)$$

The amplitude of conductance peaks can be found using the substitution, $\Delta C_g \rightarrow \Delta C_\Sigma$ in Eq. (24). The shape of the peaks can be obtained using the same substitution in the equations of Sec. III C 3 where still $\delta Q = -(C_g^{(0)} + \Delta C_g)V_g$.

B. Memory effect in current-voltage characteristics

Above we discussed the properties of SET with slow dielectric barriers, related to the variation of the gate voltage V_g at bias $V = 0$. In this subsection we instead concentrate on the current-voltage characteristic $I(V)$ of SET in the case of electron tunneling through slow insulator in the left and the right capacitors, see Fig. 1. We neglect the gate to simplify the situation, putting thus $C_g = 0$. Such systems have been extensively studied in experiments over the last two decades. They can exhibit Coulomb blockade at room temperature(21, 29–31) and their ease of fabrication makes a wide range of barrier materials available for experiments. Following Ref. 21 we consider the current-voltage characteristic of the SET in a wide range of bias voltages.

The typical current-voltage characteristics $I(V)$ are shown in Fig. 9; in Fig. 9(a)-(c) the coefficients $\Delta C_2 = 0$ and ΔC_1 are finite. It follows that there is a memory effect in $I(V)$ at large enough ΔC_1 and this effect depends on the direction of the bias voltage evolution. The jumps in plots (b) correspond to the regions of hysteresis while the arrows show the evolution of voltage. Plot (c) shows the hysteresis in $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = 3.5$. The current-voltage characteristics may have many hysteresis loops, depending on the amount of electron charge that the dielectric polarization may induce on the grain. The hysteresis in the current-voltage characteristics appears for the first time for parameter ΔC_1 being larger than $C_\Sigma^{(0)}$. This is the first critical value of polarization. For $\Delta C_1 \gtrsim 2C_\Sigma^{(0)}$ the second hysteresis loop appears in $I(V)$. Therefore this is the second critical value of ΔC_1 . For larger values of ΔC_1 we expect further increase in the number of hysteresis loops.

Two cases of current-voltage characteristics are compared in plots (e)-(d) : i) finite ΔC_1 and zero ΔC_2 and

ii) $\Delta C_1 = \Delta C_2$. In both cases the set of critical values of ΔC is the same and for large bias voltage the current-voltage characteristics asymptotically coincide.

Figure 9 shows that the current-voltage characteristics of the SET strongly depend on the direction of bias voltage V . Moreover, for a given hysteresis branch

$$I(V) \neq -I(-V) \quad (37)$$

that happens in the absence of Q , notably different from the result for a regular SET.

C. Influence on Coulomb staircase

By Coulomb staircase in this section we mean a step-like behavior of $I(V)$ in the regime of Coulomb blockade. The Coulomb staircase is often used as an indication of Coulomb blockade (Ref. 21, 29, 32–34). In the following we show how the slow polarization influences the shape of the staircase. Again we take $C_g = 0$ and, consider the conditions when the staircase is the most pronounced, i.e. $T = 0$ and strongly asymmetric barriers $R_1 \gg R_2$. At zero temperature tunneling may occur only in the direction of chemical potential drop, that is from the 1-st electrode to the 2-nd assuming $V > 0$. Due to the relatively high tunneling rate through the 2-nd electrode, the number of excess electrons on the island is almost always stays at the minimum energetically allowed number n_{\min} . It can be determined as the lowest n for which $\Delta F_2^{n+1 \rightarrow n} < 0$ is true, since $\Delta F_1^{n \rightarrow n+1} < 0$ holds for any $n < 0$. For a given n_{\min} the current can be calculated as

$$I = \frac{1}{eR_1} \Delta F_1^{n_{\min} \rightarrow n_{\min}+1}, \quad (38)$$

where ΔF_1 is the free energy change on tunneling through the 1-st electrode. For a conventional SET the above formula leads to a staircase-shaped $I(V)$ characteristic with the step width

$$\Delta V_{\text{step}} = |e|/C_1^{(0)}, \quad (39)$$

jumps of the current between the steps

$$\Delta I_{\text{step}} = |e|/R_1 C_\Sigma^{(0)}, \quad (40)$$

and the $I(V)$ slope between the jumps

$$dI/dV = C_2^{(0)}V/C_\Sigma^{(0)}R_1 \quad (41)$$

Introducing slow dielectric into the tunnel junctions result in some new effects (for the details of calculations see Appendix B). At $V > |e|/C_\Sigma^{(0)}$ slow polarization leads to the rescaling of the staircase that may be described by substituting the capacitances in Eqs. 39-41 with the new values $C_i = C_i^{(0)} + \Delta C_i$, exactly as when dealing with a conventional fast dielectric (see Fig. 10(b)). But contrary to the fast dielectric, the slow one shifts the staircase, making it asymmetric and, moreover, dependent on

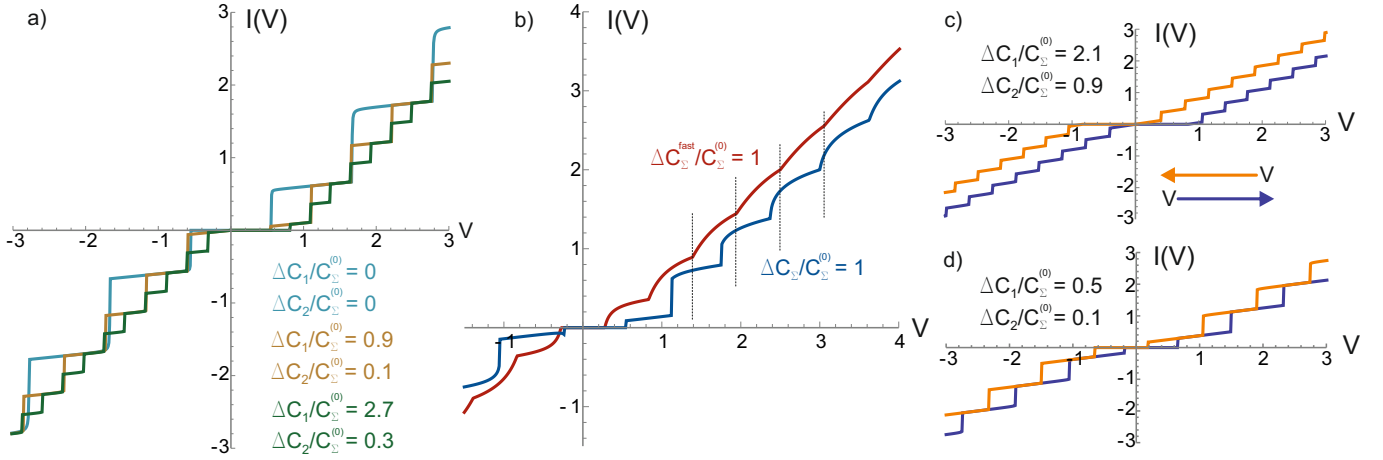


FIG. 10. (Color online) Current-voltage characteristics, $I(V)$, of SET demonstrating the Coulomb staircase at $T = 0$, $C_g = 0$. (a) $I(V)$ in the regime when the scaling of the Coulomb staircase steps at large V is the same for slow and fast dielectric response. Here $R_2/R_1 = 10^{-3}$, $C_1^{(0)} = 0.9C_\Sigma^{(0)}$, $C_2^{(0)} = 0.1C_\Sigma^{(0)}$. (b) The regime when the periods of Coulomb staircases for slow (blue curve) and fast (red curve) dielectric of the same static polarizabilities are different. $R_2/R_1 = 0.25$, $C_1^{(0)} = 0.9C_\Sigma^{(0)}$, $C_2^{(0)} = 0.1C_\Sigma^{(0)}$. (c, d) The shifts of the staircases arising from the hysteretic behavior of $I(V)$ for SET with slow dielectrics. Arrows indicate the directions of voltage change for each curve. Here $R_2/R_1 = 10^{-3}$, $C_1^{(0)} = 0.7C_\Sigma^{(0)}$, $C_2^{(0)} = 0.3C_\Sigma^{(0)}$. The unit of voltage is $|e|/C_\Sigma^{(0)}$, current is measured in $|e|/C_\Sigma^{(0)}(R_1 + R_2)$

the direction of the evolution of V , as illustrated at the Fig. 10(c,d).

Interestingly, the shift of the $I(V)$ curve in experiments is a well-known effect. It is usually accounted for by assuming the presence of some additional spurious charge Q , induced on the grain (as in Ref. 21 and 33). However the shift that we predict is notably different at least in one aspect — it reverses its sign with the direction of the evolution of V .

We stress that the described rescaling and shift of $I(V)$ takes place only under specific conditions $V > |e|/C_\Sigma^{(0)}$ and $R_1 \gg R_2$. If R_2 are of the same order the introduction of slow dielectric may change the staircase steps in a more complex way. Such a situation is shown in Fig. 10(b) where the staircase period do not correspond to the one we would expect from the simple capacitance-renormalization consideration. If R_1/R_2 is even closer to unity, the slow dielectric barriers qualitatively change the current-voltage curve as was discussed in the previous section (see Fig. 9).

V. DISCUSSION

Before discussion of specific features of our SET model, here we shortly mention limitations and possible direction of further investigations. Metallic granular is characterized by important parameter: δE — the mean spacing of single-electron levels. Here we focused on relatively large metallic granular where δE is the smallest energy parameter: $\delta E \ll T \ll E_c^{(0)}$. However, if, for example, the metallic granular diameter is 5nm or smaller and $T \sim 300K$, δE may already become comparable with

T . [Semiconductor quantum dots achieve this limit for much larger diameters.] This case has been extensively debated for SETs.³⁵ Than solving transport problem for SET with active dielectric we should take into account level statistics and calculate accordingly the statistics of peak heights in Coulomb blocked transport problem generalizing methods developed in Refs. 36–39 This calculation we leave for the forthcoming paper.

A. Requirements for dielectric materials

Here we discuss several possible dielectric materials which can be considered as slow insulators. At finite external electric field the localized electric charges are shifted and the dielectric material is polarized. There are several physical processes contributing to the polarization: 1) the shift and deformation of electron-cloud, 2) the shift of ions in the lattice, and 3) the molecular and/or macro dipole reorientation. Electrons, ions, and dipoles can form a different polarization. The slowest polarization formation corresponds to the electrocaloric and migration (electron, ion or dipole) mechanisms with the characteristic dispersion frequency being in the range $10^{-4} - 10^{-1}$ Hz and $10^{-3} - 10^3$ Hz, respectively at temperature $T = 300K$. The electromechanical mechanism corresponds to frequencies $10^5 - 10^8$ Hz, while thermal mechanism correspond to $10^5 - 10^{10}$ Hz. The dielectrics where thermal mechanism is the largest are promising for applications in nanostructures and can be considered as “slow” dielectrics.

Dithiol self-assemble monolayers (SAMs) have a static dielectric permittivity $\epsilon(\omega = 0) \sim 3$ and the character-

istic relaxation frequency $\sim 10^4$ Hz.²² These materials are good candidates for slow dielectrics. Such dielectric layers have been used in double junction SET²¹. The hysteresis have not been observed in these experiments, but there was a considerable discrepancy between the values of capacitances obtained from the fit of the experimental data with the orthodox model and the ad-initio calculations.

Another promising materials to observe the hysteresis are polar crystal dielectrics e.g., BaTiO₃ or KDP with static dielectric permittivity $\epsilon(\omega = 0) \sim 10^3$ and the typical relaxation frequency $\omega_c \sim 10^6$ Hz.

B. Fast capacitances

Here we discuss the geometric capacitance $C_i^{(0)}$, $i = 1, 2, g$. We assumed that these capacitances has an electrostatic origin. However, in rigorous analysis they include the high frequency dielectric permittivity ϵ_∞ (usually between 1 and 10). Thus in our consideration the slow polarizability α_i is the difference between the low and the high frequency α_i . As an example, for BaTiO₃ the difference between the high and low frequency permittivities ϵ is $\sim 10^3$. This difference is large enough.

C. Critical polarization

The effects of slow polarization are governed by the ratio of "slow" and "fast" capacitances $\Delta C_\Sigma / C_\Sigma^{(0)}$. If a capacitor is fully filled with a dielectric with permittivity $\epsilon(\omega)$ than $\Delta C_\Sigma / C_\Sigma^{(0)} = (\epsilon(0) - \epsilon(\infty)) / \epsilon(\infty)$. It follows from Sec. III and IV that at $\Delta C_\Sigma / C_\Sigma^{(0)} \sim 1$ the strong influence of slow polarization may be observed, thus requiring $\epsilon(0) \gtrsim 2\epsilon(\infty)$.

The latter requirement become even less strict at lower temperatures. In particular, the critical value of $\epsilon(0)^{(c)} / \epsilon(\infty)$ to observe the breakdown of conductance peaks goes to 1 as $T \rightarrow 0$ (see Eq. (36)). For the conditions as at the Fig. 8(e) $\epsilon(0)^{(c)} \approx 1.14\epsilon(\infty)$

D. Temperature dependence of the Coulomb-blockade effects

A well-known consequence from the orthodox theory of SET is that in order to experimentally observe the Coulomb-blockade phenomena, the temperature of the system should be lower than $E_c = e^2 / 2C_\Sigma$. Here the total capacitance C_Σ includes dielectric susceptibility of the barrier media. In contrast, our numerical calculations show that if the dielectric response is sufficiently slow, only the ratio $E_c^{(0)} / T$ should be taken into account when considering the blurring of the Coulomb effects due to finite temperature. This must result in more pronounced

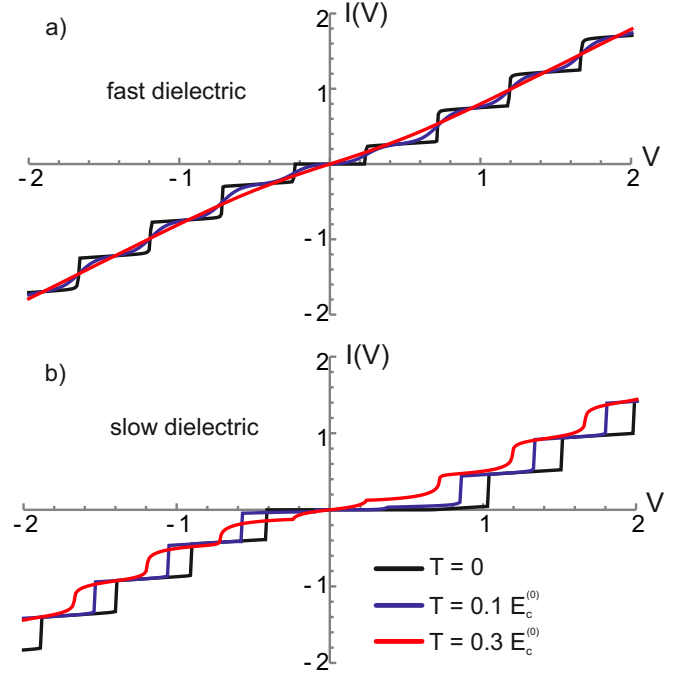


FIG. 11. (Color online). Temperature dependence of the Coulomb staircase in $I(V)$ characteristics of (a) regular SET and (b) SET with slow dielectrics in the tunnel barrier. In plot (b) the SET parameters are $C_1^{(0)} = 0.7C_\Sigma^{(0)}$, $C_2^{(0)} = 0.3C_\Sigma^{(0)}$, $\Delta C_1 = 1.4C_\Sigma^{(0)}$, $\Delta C_2 = 0$. In plot (a) $C_1 = 2.1C_\Sigma^{(0)}$ and $C_2 = 0.3C_\Sigma^{(0)}$. For both plots $R_2/R_1 = 10^{-3}$ and in (b) $I(V)$ is shown for increasing voltage V . The unit of voltage is $|e|/C_\Sigma^{(0)}$, the current is measured in $|e|/C_\Sigma^{(0)}(R_1 + R_2)$

blockade for a system with slow dielectric at a given temperature and electrode geometry, as illustrated in Fig. 11.

VI. CONCLUSIONS

We showed that the dielectric materials at the nanoscale demonstrate new physical phenomena. As an example we studied the single-electron transistor. We found the memory effect in the conductance-gate voltage dependence and in the current-voltage characteristics of the SET. We uncovered the complex fine structure of the hysteresis-effect, where the "large" hysteresis loop may include a number of "smaller" loops. We also found, that in order to estimate the influence of temperature on the electronic transport one should compare T with $e^2 / 2C_\Sigma^{(0)}$ where in $C_\Sigma^{(0)}$ the slow part of the dielectric function is not included.

ACKNOWLEDGMENTS

N.C. acknowledges for the hospitality Laboratoire de Physique Thorique, Toulouse where this work was final-

ized and CNRS. S. F. was supported by Russian National Foundation (Grant No. RNF 14-12-01185), N.C. by Russian Foundation of the Basic Research (grant No. 13-02-0057), the Leading Scientific Schools program No. 6170.2012.2 and SIMTECH Program, New Centre of Superconductivity: Ideas, Materials and Technologies (grant No. 246937). I.B. was supported by NSF under Cooperative Agreement Award No. EEC-1160504, NSF Award No. DMR-1158666, and the NSF PREM Award.

Appendix A: Calculation of the Coulomb energy change on electron jumps

Here we show, how the energy changes ΔU_n^\pm are calculated. If the number of electrons on the island changes from n to $n \pm 1$ in some process, than the electrostatic energy change is

$$\Delta U_n^\pm = \int_n^{n\pm1} \sum_i (\phi - V_i) dq_i = \int_n^{n\pm1} \sum_i (\phi - V_i) (C_i^{(0)} d\phi + S_i dP_i), \quad (\text{A1})$$

where q_i are the charges of the capacitors and P_i are dielectric polarizations in barriers. For fast and slow dielectrics P_i behave differently during the process of electron jump. If dielectric response is fast P_i follows ϕ that results in capacitance renormalization. For slow dielectric layers the polarization cannot change on the electron jump timescale and thus $dP = 0$ yielding

$$\Delta U_n^\pm = \frac{1}{2} \sum_i C_i^{(0)} (\phi - V_i)^2 \Big|_{\phi(n)}^{\phi(n\pm1)}. \quad (\text{A2})$$

$\phi(n)$ are calculated using the charge balance equation (3)

$$\phi(n) = \frac{1}{C_\Sigma^{(0)}} \left[e \left(n - \sum_i P_i S_i / e \right) + \sum_i C_i^{(0)} V_i \right]. \quad (\text{A3})$$

Here P_i are constant and do not depend on n . By inserting Eq. (A3) into (A2) we obtain Eq. (9).

Appendix B: The shape of the Coulomb staircase

At zero temperature the tunneling rates for the electron to and from the island are

$$\Gamma_{1,2}^{n \rightarrow n\pm1} = \frac{1}{e^2 R_{1,2}} (-\Delta F_{1,2}^{n \rightarrow n\pm1}) \Theta (-\Delta F_{1,2}^{n \rightarrow n\pm1}), \quad (\text{B1})$$

where n is the number of excess electrons on the island and tunneling happens through the 1-st or the 2-nd electrode. Free energy changes $\Delta F_{1,2}$ on jumps are

$$\Delta F_1^{n \rightarrow n\pm1} = \frac{e}{C_\Sigma^{(0)}} \left(\frac{e}{2} \pm (ne - Q') \pm C_2^{(0)} V \right) \quad (\text{B2})$$

$$\Delta F_2^{n \rightarrow n\pm1} = \frac{e}{C_\Sigma^{(0)}} \left(\frac{e}{2} \pm (ne - Q') \mp C_1^{(0)} V \right). \quad (\text{B3})$$

Consider $V > 0$. It follows from B1 that tunneling occurs if for some n simultaneously $\Delta F_1^{n \rightarrow n+1} \leq 0$ and $\Delta F_2^{n+1 \rightarrow n} \leq 0$ (there is no backward tunneling at $T = 0$). These conditions may be combined into

$$Q'/e - 1/2 + C_1^{(0)} V/e \leq n \leq Q'/e - 1/2 - C_2^{(0)} V/e. \quad (\text{B4})$$

Since the tunneling from the 1-st electrode to the island is much slower than from the island to the 2-nd electrode ($R_1 \gg R_2$), the number of electrons on the island almost constantly stays at it's lowest energetically allowed value n_{\min} . The current is, than,

$$I = -e \frac{\Gamma_1^{n \rightarrow n+1} \Gamma_2^{n+1 \rightarrow n}}{\Gamma_1^{n \rightarrow n+1} + \Gamma_2^{n+1 \rightarrow n}} \approx -e \Gamma_1^{n_{\min} \rightarrow n_{\min}+1}. \quad (\text{B5})$$

The rest is to calculate n_{\min} . Since we neglect C_g only the charge induced by the slow polarization gives rise to Q'

$$Q' = \frac{\Delta C_\Sigma}{C_\Sigma} n_{\min} e + \frac{\Delta C_1 C_2^{(0)} - \Delta C_2 C_1^{(0)}}{C_\Sigma} V. \quad (\text{B6})$$

n_{\min} can be determined from the equation

$$\left[-\frac{1}{2} - \frac{n_{\min}}{1 + \Delta C_\Sigma / C_\Sigma^{(0)}} + \frac{C_1}{(1 + \Delta C_\Sigma / C_\Sigma^{(0)})} \frac{V}{e} \right] = 0, \quad (\text{B7})$$

where $[x]$ denote the lowest integer bigger than x . It worth noting that the equation B7 predicts multiple solutions for n_{\min} at V close to the current jump points if $\Delta C_\Sigma > 0$ (see Fig. 10(d)).

The calculation of I yields

$$I(V) = \frac{1}{R_1 C_\Sigma} \left(\frac{e}{2} \frac{C_\Sigma}{C_\Sigma^{(0)}} + n_{\min} e + C_2 V \right). \quad (\text{B8})$$

The latter formula demonstrates the full renormalization of capacitances and a shift in the $I(V)$ as is illustrated at the Fig. 10(a).

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