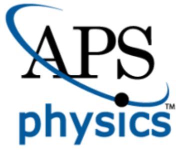

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Characterization of Low Frequency Noise in the Resistive Switching of Transition Metal Oxide HfO_2

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Abstract - Low frequency noise measurements were performed on HfO_2 based bipolar resistive switching memory devices. A $1/f^{\alpha}$ DC noise power spectral density was observed with α~1 for low resistance state and α~2 for high resistance state. We developed an electron tunneling model to elucidate the conduction process which showed that the $1/f^{\alpha}$ behavior was due to the distribution of relaxation times of electron tunneling between the electrodes and the traps in the conducting filaments. The transition of the slope index α from 1 to 2 at a certain cutoff frequency indicates that there is a tunneling gap formed between electrodes and the residual of the conductive filaments in the high resistance state.

Keywords – low frequency noise, resistive switching (RRAM), transition metal oxide, electron tunneling

In recent years, resistive switching phenomena have been widely observed in transition metal oxides such as $Pr_{0.7}Ca_{0.3}MnO_3$ [1], $SrTiO_3$ [2], NiO [3], TiO_2 [4], Cu_2O [5], ZnO [6], HfO_2 [7], ZrO_2 [8], etc. Currently, transition metal oxide based resistive switching memory is extensively studied as one of the most competitive candidates for future non-volatile memory applications due to its simple structure, fast switching speed, great scalability, and compatibility with silicon complementary metal-oxide-semiconductor (CMOS) technology [9-11]. The mechanism of resistive switching phenomenon in oxides is usually attributed to the formation/rupture of conductive filaments (CFs) which may consist of oxygen vacancies or metal precipitates [12]. The set process from high resistance state (HRS) to low resistance state (LRS) is interpreted as a dielectric soft breakdown associated with the migration of oxygen ions toward the anode, leaving behind the oxygen vacancies in the bulk oxide to form CFs connecting both electrodes [13]. To reset from LRS to HRS, there are two modes: in the unipolar reset (the reset occurs at the same polarity as the set), Joule-heating-assisted diffusion of oxygen ions from anode and surrounding oxides rupture the CFs by recombination with oxygen vacancies or re-oxidization of the metal precipitates [14]. In the bipolar reset (the reset occurs at the opposite polarity as the set), electric-field-assisted drift of oxygen ions from the oxygen reservoir rupture the CFs [15]. In the bipolar switching mode, oxidizable electrode materials such as Ti, TiN, TaN are usually used to serve as the oxygen reservoir providing the oxygen ions during the reset process [16]. The device used in this paper exhibits the bipolar switching mode. Although such a phenomenological physical switching picture above has been proposed, the detailed characterization and quantitative theoretical analysis of the conduction mechanism is still lacking in the literature.

Low frequency noise (LFN) measurement is a technique that can electrically characterize the trap-assisted conduction process in dielectrics [17-19]. A $1/f^{\alpha}$–like power spectral density (PSD) has been observed for different resistive switching memory devices such as $Pr_{0.7}Ca_{0.3}MnO_3$ [20], TiO_2 [21], NiO [22] (in this paper f refers to the frequency). In this work, we perform LFN measurement on HfO_2 based resistive switching memory to investigate its conduction and switching mechanism. HfO_2 is chosen because HfO_2 based devices exhibit desirable properties such as ultra-fast switching speed (<ns), excellent switching endurance (>10^{10} cycles), and reliable data retention (10 years extrapolated at 200 °C) [23], and 4 Mb memory circuit array has been demonstrated with a potential for large scale manufacturing [24]. By analyzing the $1/f^{\alpha}$–like data, we find a distinct slope index α for LRS and HRS, and the slope transition at the cutoff frequency indicates a tunneling gap formation between the electrodes and traps in the CFs in HRS.

Resistive switching stack of $TiN/HfO_2/Al_2O_3/Pt$ thin films were fabricated. TiN is the top electrode and Pt is the bottom electrode. The oxide matrix consists of HfO_2/Al_2O_3, HfO_2 is the active switching layer, and the purpose of embedding a buffer Al_2O_3 layer is to improve the switching uniformity [25]. 50 nm Pt was first deposited by e-beam evaporation on silicon substrate. Then 5 nm Al_2O_3 was deposited by atomic layer deposition (ALD) using TDMA-Al (tetrakis dimethylamido aluminum $Al[N(CH_3)_2]_4$) and H_2O as

precursors at 300 °C, and then 5 nm HfO_2 was deposited by ALD using TEMA-Hf (tetrakis ethylmethylamino hafnium $Hf[N(C_2H_5)(CH_3)]_4$) and H_2O as precursor at 220 °C. The crossbar patterns with 0.5×0.5 μm^2 active cell area were defined by photolithography. Then 50 nm TiN was deposited by reactive sputtering and was lifted-off. Agilent 4156C semiconductor parameter analyzer was used to measure the DC switching characteristics and provide the DC bias for noise measurement. The noise current was fed into in a Stanford Research System SR 570 low noise amplifier, and the output signals were analyzed by a Stanford Research System SR 760 spectrum analyzer. The electrical measurement was done in a shielded environment. The bottom electrode (Pt) was grounded and the bias was applied to the top electrode (TiN) in all the measurements. More information about the measurement methodology can be found in the supplementary materials of this paper. A schematic diagram of the connection of the instruments is shown in Fig. 1S in the supplementary materials [26]. And the noise floor of the measurement system was measured to be around 10^{-22} A^2/Hz for LRS and 10^{-24} A^2/Hz for HRS. In either case, the noise level of the system was more than 3 orders lower than that of the memory devices when they were biased at 0.3 V, as shown in the Fig. 2S in the supplementary materials [26]. Therefore, the effect the measurement system is negligible.

Fig. 1 (a) shows the bipolar switching characteristics of our samples. After an initial high voltage (~ 10 V) “electroforming” process [27], the devices are active and can switch reversibly between LRS and HRS. With the increase of the applied positive voltage (0 V→3 V), the current suddenly jumps after some critical voltage and then the device switches from HRS to LRS. This process is typically called “set”. A compliance current (100 μA) is forced by the semiconductor parameter analyzer to limit the current in order to prevent the hard breakdown of the device, thus the current is fixed to be 100 μA through a feedback loop of the semiconductor parameter analyzer. Then the voltage is swept back (3 V → 0 V) and the LRS current usually follows a linear I-V relation. Next with the increase of the applied negative voltage (0 V → -3 V), the current gradually drops after some critical voltage and then the device switches from LRS to HRS. This process is typically called “reset”. Then the voltage is swept back (-3 V → 0 V), and the HRS current usually shows super-linear I-V relation. Other performance parameters of our samples such as switching speed (~10 ns), endurance (~10^6 cycles), retention (>2 hours @ 100 °C) and multilevel resistance states capability by controlling reset voltages were reported in previous publications [28-29]. Fig. 1 (b) shows the relative noise current fluctuation in the time domain for different resistance states. The higher HRS levels can be obtained by increasing the reset stop voltages in a DC sweep. Generally, the higher the resistance state is, the larger the relative fluctuation is. Fig. 2 (a) shows the normalized PSD (S_i/I^2) in the frequency domain for different resistance states. Here the normalization is done by dividing the PSD value (S_i) by the square of the average current (I^2). It is seen that the higher the resistance state is, the larger the normalized PSD is, which is in agreement with the data in the time domain. Also from Fig. 2 (a), it is seen that for LRS the slope index α is close to 1, while for HRS there is a cutoff frequency above which α changes from 1 to 2. Similar LFN behavior that shows a slope index change was also observed in other resistive switching

memory devices [20, 21, 30]. Fig. 2 (b) shows the PSD (S_i) as a function of the squared DC bias for LRS (the inset) and HRS respectively. It is seen that the PSD (S_i) in LRS follows a linear relation with the squared DC bias while that in HRS follows a super-linear relation with the squared DC bias, which is consistent with the I-V relation in Fig. 1 (a). As a result, the normalized PSD (S_i/I^2) for both HRS and LRS are almost independent of the DC bias as shown in Fig. 2 (c), suggesting that there is no optimal bias point for maximum signal to noise ratio (SNR) for the read operation.

In the following, we discuss the conduction and switching mechanism that is revealed by the above LFN characterization. Previous studies suggested that the conduction in HfO_2 based resistive switching memory is dominated by trap-assisted-tunneling process based on the observation that the measured current is insensitive to the temperature change [31-32] and a rise of the AC conductance under high frequency external signal stimulus [33]. The $1/f^{\alpha}$ noise measured in this work also has a very weak dependence of the temperature (see the Fig. 3S in the supplementary materials [26]). Oxygen vacancies that are created during the forming process can serve as the traps for conduction. In LRS, the conductive filaments (CFs) with oxygen vacancies connect both electrodes, while in HRS, the CFs are ruptured near one electrode (the electrode that is biased negative during the reset process) and a gap region poor in oxygen vacancies is formed (see Fig. 3 (a) for the illustration). The trap-assisted-tunneling consists of electrode-to-trap tunneling and trap-to-trap tunneling. It has been pointed out [34] that electrode-to-trap tunneling is the bottleneck of the DC conduction process for the following two cases: 1) the electron injection is limited by a significant interfacial potential barrier as the case of metal/oxide interface, leading to a slow electrode-to-trap tunneling rate; 2) the trap density of the remaining un-ruptured section of the CFs is high, leading to a fast trap-to-trap tunneling rate within the residual CFs. The DC noise current of the resistive switching memory stack is usually attributed to be a random trap/detrap process through the defects such as oxygen vacancies in the CFs [35-36] with a relaxation time τ. The relaxation time, τ, is determined by the transition time for electrode-to-trap tunneling because the trap-to-trap hopping rate is much larger than the electrode-to-trap tunneling rate [32]. The Wentzel-Kramers-Brillouin (WKB) approximation [37] is used to calculate this τ as Eq. 1.

$$\tau = \tau_0 / f_{\mathrm{Fermi-Dirac}}(E_b - E_t) \cdot \exp(\gamma \cdot d) \quad (1)$$

where d is the distance from electrode to trap, τ_0 is the pre-exponential time factor (~10^{-14} s [38]), $\gamma = 2\sqrt{2m^* E_t}/\hbar$ is the WKB approximation factor for the transmission probability at low bias, trap energy E_t=1.6 eV [39] in HfO_2, TiN/HfO_2 interface potential barrier E_b=1.9 eV [40], and effective mass $m^*=0.1m_0$ for HfO_2 [39]. For a specific τ, the PSD of the noise current $S_i(\omega)$ can be expressed in a Lorentzian function as Eq. 2 [17-19].

$$S_i(\omega) = \overline{(\Delta I)^2} \cdot \frac{4\tau}{1+\omega^2\tau^2} \quad (2)$$

where $\omega=2\pi f$ is the angular frequency, $\overline{(\Delta I)^2}$ is the root mean square (RMS) value of the noise current. And if the τ has a probability distribution p(τ), the PSD form is modified to be Eq. 3.

$$S_i(\omega) = \int_{\tau(\min)}^{\tau(\max)} \overline{(\Delta I)^2} \cdot \frac{4\tau}{1+\omega^2\tau^2} \cdot p(\tau)\, d\tau \quad (3)$$

where τ(min) is the relaxation time determined by the shortest tunneling distance, and τ(max) can be considered to be infinite if we consider the direct tunneling from one electrode to another across entire 10 nm thick oxide is negligible.

Fig. 3 (a) shows the schematic of the conduction process in LRS and HRS. Fig. 3 (b) shows the Lorentzian function for different electrode-to-trap tunneling distances. In LRS, CFs connect both electrodes, thus electrons can tunnel from the electrode to all the traps nearby with various relaxation times. If we assume a spatially uniform distribution of traps in LRS, $p(R) = n_t \cdot 4\pi R^2$, with a trap density n_t, by changing the integration variable: $p(\tau) = p(R) dR/d\tau$, we can complete the integration at the limit when τ(min) is approaching zero for the case of LRS, and obtain the result of Eq. 4.

$$S_i(\omega) = \overline{(\Delta I)^2} \cdot 8\pi^2 n_t/\gamma \cdot R_\omega^2/\omega \quad (4)$$

where $R_\omega = 1/\gamma \cdot \ln(1/\omega\tau^0_{e-t})$ is the characteristic tunneling distance at frequency ω, which has only a weak dependence on ω. With respect to the frequency, $S_i(\omega) \sim 1/\omega^\alpha$, here the slope index $\alpha = 1 + 2/\ln(1/\omega\tau)$, since $\omega\tau \ll 1$ at the LFN regime ($f < 3$ kHz), α approaches 1. Intuitively speaking, in LRS the electrons have multiple choices when they tunnel from the electrode to the traps nearby (see Fig. 3 (a)), and the contribution from all these transitions will smooth the $1/f^2$ Lorentzian function thus the envelope leads to $1/f^\alpha$-like ($\alpha \sim 1$) LFN behavior (see Fig. 3 (b)). In HRS, CFs are ruptured and the shortest distance between the first trap and the electrode causes a minimum τ (see Fig. 3 (a)), thus $\omega = 1/\tau_{(min)}$ corresponds to the cutoff frequency in the Lorentizian (see Fig. 3 (b)). Therefore, the cutoff frequency becomes an indicator of the ruptured CFs length. In Fig. 3 (c), the tunneling gap distances are roughly estimated for the three HRS levels shown in Fig. 2 (a) according to their cutoff frequencies. It is seen that a higher resistance shows a lower cutoff frequency and indicates a larger tunneling transition time, thus corresponding to a lager tunneling gap distance. For a typical HRS range (500 kΩ-50 MΩ), the ruptured CFs length is estimated to be 1.5 nm-2 nm. To probe the extremely high HRS range (>50 MΩ), ultra-low frequency (<10 Hz) noise measurement and further decreasing the measurement system noise floor is needed, which is beyond our measurement system's limit. The above physical picture was inspired by the McWhorter model [41]. The McWhorter model was initially developed to explain the low frequency noise spectrum in the drain current of the field-effect transistor. The tunneling of electrons to the interfacial traps in the gate dielectric with different tunneling distances would cause a fluctuation of the number of electrons in the channel, which manifest as the *1/f* noise in the drain current. The main difference between the McWhorter model and our proposal for the resistive switching memory devices is that in the McWhorter model, the tunneling paths of the electrons into or out of the gate dielectric is perpendicular to the current flowing direction in the channel, while in the resistive switching memory the tunneling paths of the electrons are along with the current flowing direction. In fact, the trap/detrap processes determine the steady state current and the randomness of the trap/detrap processes give rise to the noise current on top of the steady state current in the resistive switching memory devices.

In summary, $1/f^\alpha$ behavior of the LFN was observed in HfO_2 based resistive switching memory. The

LFN behavior is attributed to the distribution of relaxation time of electron tunneling between the electrode and the traps in the CFs. The slope index α approaches 1 for LRS because multiple transition with various relaxation times is allowed, and α changes to 2 for HRS at the cutoff frequency because the shortest tunneling path cause a minimum relaxation time. From the LFN characterization, it is suggested that the switching between LRS and HRS is due to a formation of tunneling gap by partially rupturing the CFs. This paper provides new characterization methods and deeper understanding of the physics of resistive switching in transition metal oxides.

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Figure Caption:

Fig. 1 (a) Typical bipolar I-V characteristics of $TiN/HfO_2/Al_2O_3/Pt$ resistive switching memory device. The I-V in LRS is almost linear while the I-V in HRS is super-linear (the inset).

Fig. 1 (b) Noise current at 300 mV DC bias in the time domain for different resistance states. 300 mV is chosen because it is small enough to avoid unintentional disturbance of the resistance states and it is large enough to give a measurable current level. The higher the resistance state is, the larger the relative noise current fluctuation ($\Delta I/I$) is.

Fig. 2 (a) The $1/f^{\alpha}$-like normalized PSD (S_i/I^2) for different resistance states. The higher the resistance is, the larger the normalized PSD is. From LRS to HRS, the slope index α changes from 1 to 2 at a certain cutoff frequency.

Fig. 2 (b) The PSD (S_i) in LRS (the inset) and in HRS as a function of the DC bias voltage. The PSD (S_i) in LRS increases in a way similar to the linear I-V relation in LRS, and the PSD (S_i) in HRS increases in a way similar to the super-linear I-V relation in HRS.

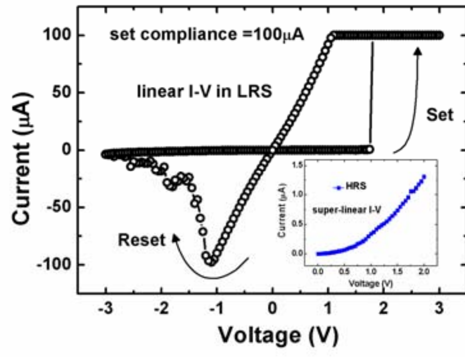
Fig. 2 (c) The normalized PSD (S_i/I^2) as a function of the DC bias voltage. For both LRS and HRS, the normalized PSD (S_i/I^2) is almost independent on the bias, suggesting there is no optimal bias point for maximum signal to noise ratio (SNR) in read operation.

Fig. 3 (a) Schematic of the conduction process in resistive switching memory: in LRS, the electrons have multiple tunneling paths with various relaxation times while in HRS, the shortest tunneling path causes a cutoff frequency in the LFN behavior.

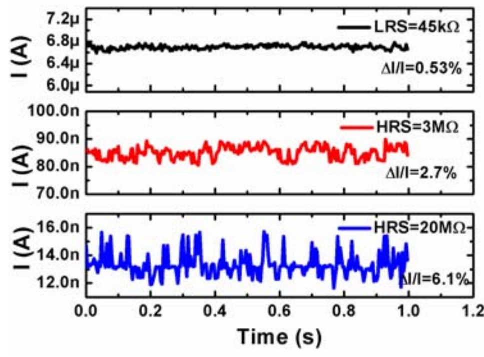
Fig. 3 (b) Lorentzian function $4\tau/(1+\omega^2\tau^2)$ for different τ. Single Lorentzian is $1/f^2$, and the envelope of multiple Lorentzian is $1/f$. The cutoff frequency corresponding to a shortest electrode-to-trap tunneling gap distance (~2 nm) is shown (the dash line).

Fig. 3 (c) The observed cutoff frequency and the estimated tunneling gap distance for the three HRS levels shown in Fig. 2 (a).

Fig. 1

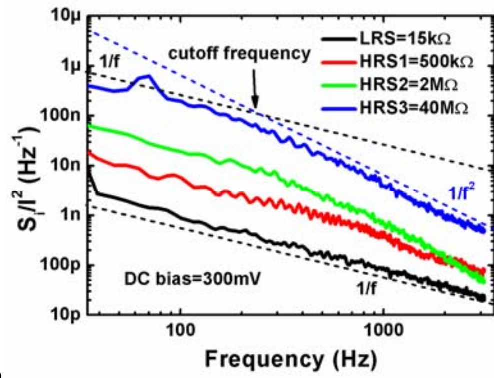


(a)

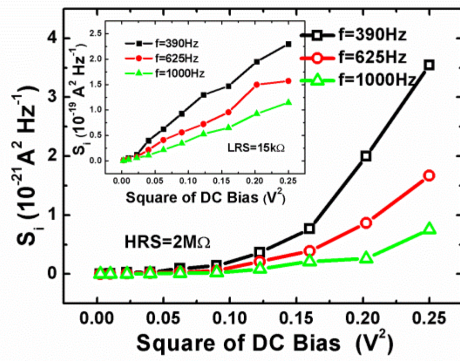


(b)

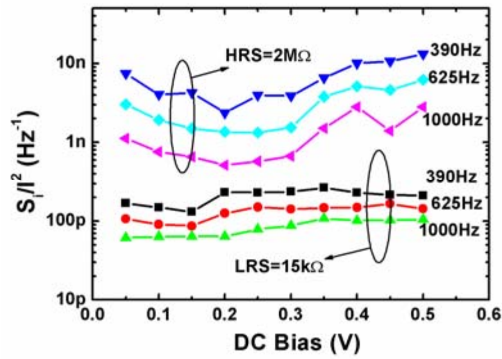
Fig. 2



(a)

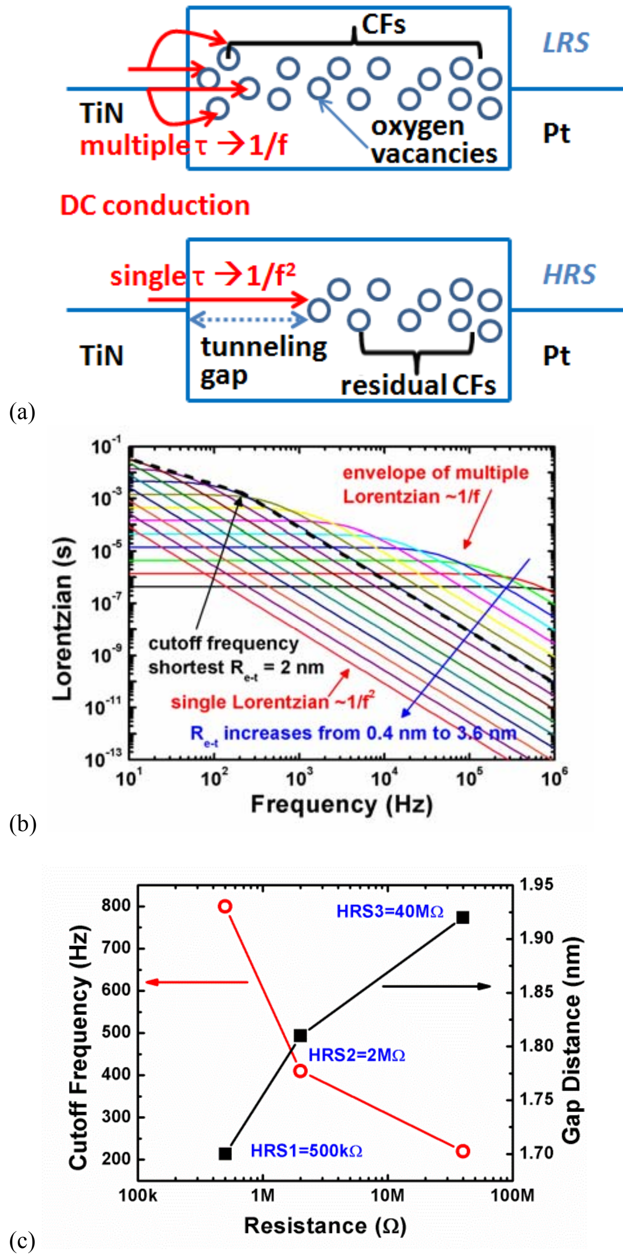


(b)



(c)

Fig. 3



(a)

(b)

(c)