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Tunneling, Current Gain, and Transconductance in Silicon-Germanium Heterojunction Bipolar Transistors Operating at milliKelvin Temperatures

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Abstract

Quantum transport measurements in advanced Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs) are presented and analyzed, including tunneling spectroscopy of discrete impurity levels localized within the transistor and the dependence on an applied magnetic field. The collector current at mK temperatures is well accounted for by ideal electron tunneling throughout the entire base. The amplification principle at mK temperatures is fundamentally quantum mechanical in nature: an increase in base voltage, requiring a moderate base current, creates an equal and opposite decrease in the tunneling barrier seen by the electrons in the emitter, thereby increasing the collector current significantly more than the base current, producing current gain. Highly-scaled SiGe HBTs operate predictably at mK temperatures, thus opening the possibility of viable SiGe mK circuitry.

Amplification of weak electronic signals sourced at mK temperatures is important for single-shot qubit readout circuits, [1–3] electron counting in metrology, [4, 5] single-photon counting in the far-infrared, [6] and for the detection of micromechanical motion near the quantum ground-state. [7] Since the discovery of modulation-doped semiconductor heterojunctions, [8] the high electron mobility transistor (HEMT) is perhaps the most studied cryogenic transistor, [9] and has been used at 4 K, [10, 11] 1 K, [12] and 100 mK temperatures. [13–15] The principal reason for its attractiveness for low temperature operation is that the channel electrons remain highly mobile down to the lowest (mK) temperatures and can be modified by an electric field applied by a gate lead. But this property of the HEMT is also its main drawback, because it is difficult to manufacture robust capacitively coupled gates capable of depleting carriers at the nanometer-scale. In addition to HEMTs, other, more specialized, cryogenic amplifiers have been devised, including radio-frequency reflectometers, [3, 16, 17] and Josephson parametric amplifiers. [7, 18–21] In comparison, conventional (homojunction) bipolar junction transistors (BJTs) have generally not been used in cryogenic applications, due to their strong degradation in current gain (via bandgap narrowing), parasitic resistance (carrier freeze-out), and frequency response (carrier diffusivity) at low temperatures. [22]

In the present article we revisit the physics of BJTs operating at mK temperatures for the case of modern SiGe HBTs, which are essentially Si BJTs that have been bandgap engineered for enhanced (room temperature) performance. It is well known that SiGe HBTs have excellent cryogenic properties, and aggressive scaling further accentuates their desirable properties at deep cryogenic temperatures. [23–26] At low values of power dissipation, SiGe HBTs still have useful gain, low-noise, and good frequency response, [27–29] suggesting that the physical properties of SiGe HBTs should be further investigated and understood at mK temperatures. In the absence of thermally-generated carriers at mK temperatures, the classical drift-diffusion picture of charge transport in the transistor becomes inapplicable, and there remains a fundamental question of how such transistors can amplify in the quantum regime. The purpose of the present article is to give a comprehensive evaluation and account of charge transport and amplification in SiGe HBTs at mK temperatures, in best-of-breed, 4th-generation devices. As will be shown, we arrive at a picture of electron transport at mK temperatures in which the collector current at low bias is reasonably well accounted for by ideal quantum mechanical tunneling through the entire base region, where

electrons tunnel directly from the emitter into the collector. The transconductance is then determined by the shift of the tunneling barrier height and width in the neutral base with base-emitter voltage. The observed base current is due to less understood processes. But as long as the collector current is well accounted for by the model and much higher than the base current, understanding of the base current is not as important for many circuit applications. This new understanding of the collector current can provide a useful starting point for designing SiGe HBT amplifiers for mK temperatures.

The article is organized as follows. In Section I we discuss the experimental setup used, while in Sections II, III, and IV we present measurement results integrated with discussions of the transport simulations. Finally, in Section V we discuss possible applications and emphasize the importance of high performance SiGe-HBTs for circuits operating at mK.

I. EXPERIMENTAL SETUP

The SiGe HBT investigated in this work is from the GlobalFoundries fourth-generation, 90-nm SiGe BiCMOS technology (GF 9HP), with a BV_{CEO} of 1.7 V and f_T/f_{max} of 300/360 GHz at 300 K. [30] Three devices were measured. Samples 1 and 2 have an emitter geometry of $0.1 \times 4.0\mu\text{m}^2$ ($0.1 \times 2.0\mu\text{m}^2$ in sample 3).

Figure 1 displays scanning electron micrographs (SEMs) and schematic cross-sections of the device. The three contacts (emitter, base, and collector) are all ohmic contacts. As shown in the cross- section of figure 1**a**, the base contact is formed by first extending the intrinsic base (the portion below emitter) to a highly doped extrinsic base (the portion right above shallow trench isolation STI), before contacting the tungsten plug (grey metal). Collector contact is formed by highly doped n+ sub-collector and reach-through. The emitter contact is a highly-doped polysilicon pillar right above the n-region. There is no Schottky barrier in the device. There are oxide-passivated edges between the emitter and extrinsic base, which are known as the EB spacer. Figure 1**b** shows the circuit diagram used in characterization of the HBTs. The close-up image of the HBT is shown in figure 1**c**. Letter S indicates the silicon dioxide EB-spacer. The intrinsic base is approximately 25nm in width. Figure **d** shows the schematic of the device. The yellow portion is a nitride used in the self-alignment process, and EB-spacer is the small (barely visible) red-oxide portion directly under that.

Measurements were performed using a Quantum Design Physical Property Measurement

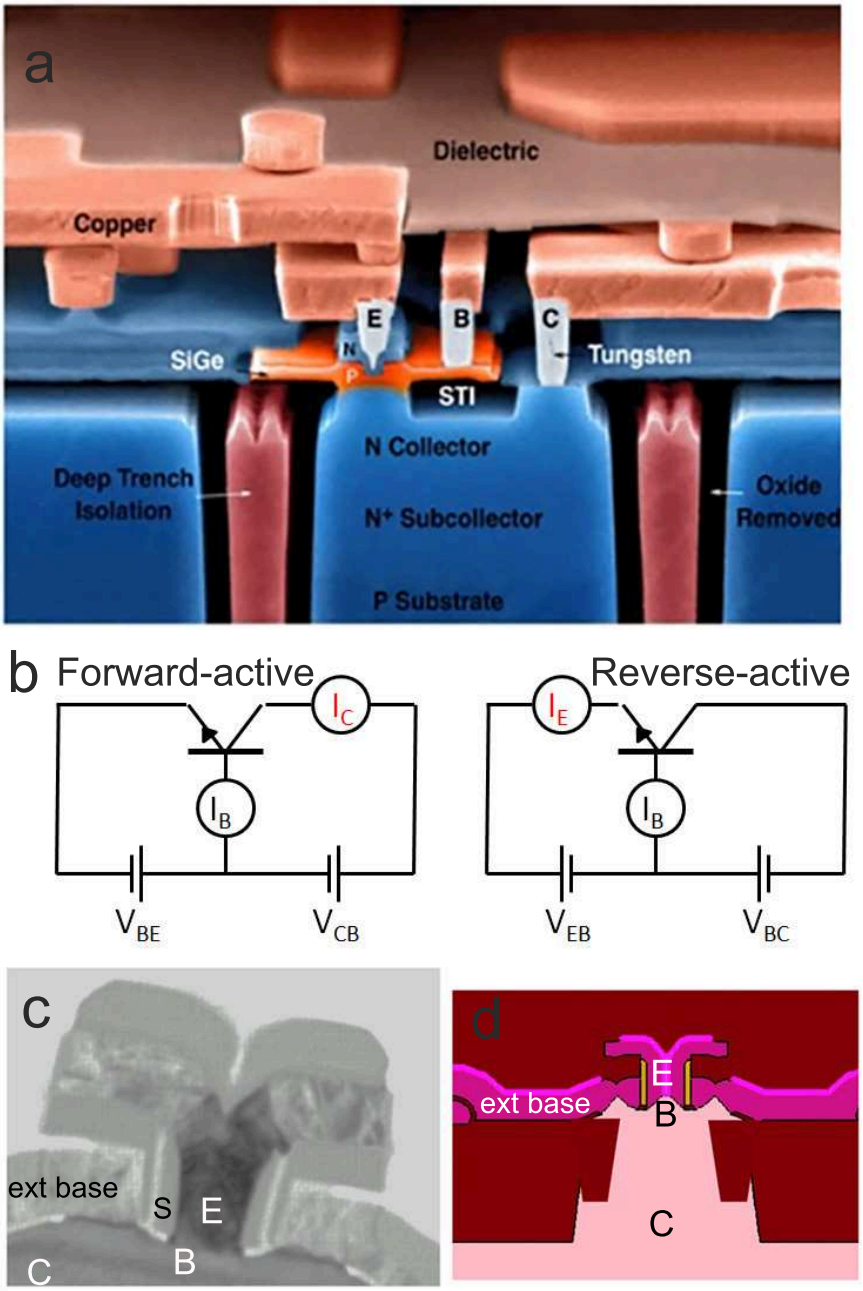

FIG. 1. A 90nm SiGe BiCMOS Technology for mm-wave and high-performance analog applications. **a**: Scanning electron micrograph of the SiGe-HBT device. **b**: Schematic of the circuits used to characterize an HBT-device. **c**: Close-up scanning electron micrograph of the HBT, showing the polysilicon emitter (E), intrinsic epitaxial base (B), extrinsic polysilicon base, the epitaxial collector (C), and the silicon dioxide EB-spacer (S). **d**: Schematic of the HBT. The vertical yellow portion is the silicon nitride used in the self alignment process.

System (PPMS) DynaCool system with a dilution refrigerator (DR) insert. The collector current changes by up to ten-orders of magnitude at a given temperature. To simplify the measurements over such a wide current range, we used an Agilent 4156C Semiconductor Parameter Analyzer (4156C). The minimum voltage step and voltage resolution of the 4156C are 0.1 mV and 2 μV, respectively. For heat sinking, the samples were attached to the PPMS gold packages using indium solder. Electrical connections between the die and package were made with gold wirebonds. The package was placed in the DR insert and the electrical connections to room temperature Fischer-connectors were aluminum twisted pairs. No additional cryogenic filtering was applied. For the room temperature electronics, the Fischer connector was adapted to triaxial cabling into the 4156C to reduce noise. The DR base temperature is 50 mK, and the nominal cooling power at 100 mK at the sample location is 0.25μW.

During the experiment, we observed the temperature increase due to samples heat dissipation at collector current > 1 μA, measured using the dilution refrigerator thermometry. To reduce the effects of elevated ambient temperature on the validity of measurements, an aggressive (fast) DC sweep was performed up to 1 mA collector current. This allowed us to obtain the device characteristics before the ambient temperature is changed by more than 50 mK from its nominal condition.

II. GUMMEL CHARACTERISTICS

The quasi-exponential dependence of the collector and base currents on base-emitter voltage is well visualized using the Gummel characteristics (i.e., the log of the collector and base currents on linear base-emitter voltage). The forward-active mode (normal) and the reverse-active mode (emitter and collector electrically swapped) Gummel characteristics of the three samples are shown in Figs. 2**a**,**c**,**e** and **b**,**d**,**f**, respectively. The circuit diagrams for these two operational modes are shown in figure 1**b**. Usually in the transistor circuit in the forward-active mode $V_{BE} > 0$ and $V_{CB} > 0$. With modern transistors that typically have large current gain, it is quite possible to operate the transistor at saturation mode ($V_{CB} \leq 0$) and still have enough current gain for a circuit application. Because collector doping profiles are often different for devices on the same wafer (some optimized for high speed, while others are optimized for high breakdown voltage), it is common practice to characterize transistor

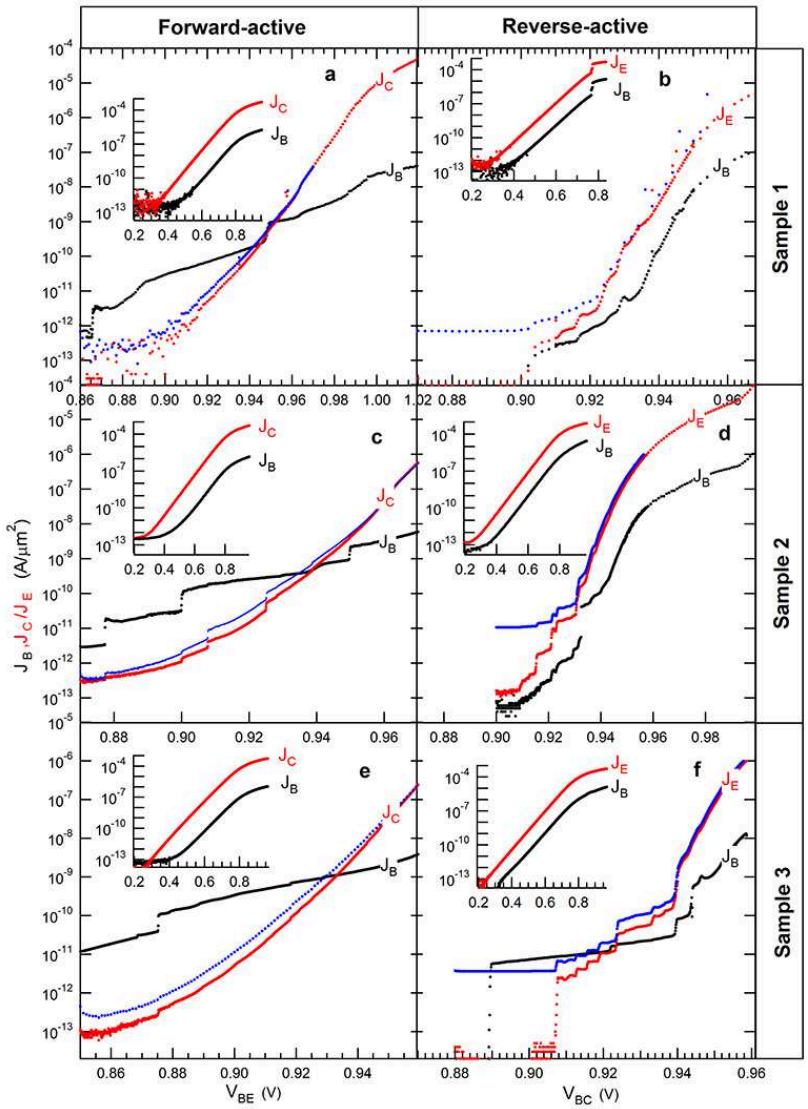

FIG. 2. Gummel characteristics measured in three devices at $T = 70$ mK: **a**, **c**, and **e** correspond to the forward-active mode in samples 1, 2, and 3, respectively. **b**, **d**, and **f** correspond to the reverse-active mode in samples 1, 2, and 3, respectively. The upper left insets display the corresponding Gummel characteristics measured at room temperature. The circuit schematics for the forward-active and reverse-active mode is shown in figure 1**b**. **a**, **c**, and **e**: Red and black dots correspond to respective collector and base current densities at $V_{CB} = 0$. Blue dots correspond to the collector current density at $V_{CB} = 0.5$ V. The base current density at $V_{CB} = 0.5$ V is indistinguishable from that at $V_{CB} = 0$. **b**, **d**, and **f**: Red and black dots correspond to respective emitter and base current densities at zero V_{EB}, blue dots corresponds to the emitter current density at $V_{EB} = 0.2$ V.

behaviors at $V_{CB} = 0$, thus removing all transport between base and collector due to junction bias. This reduces the transport to carriers initiated from emitter, and provides a good baseline for comparison between different devices and technology platforms. We adopted such a practice in the measurements described here as well (e.g., the base and collector are biased at the same potential ($V_{CB} = 0$)). Thus, while in that case $dJ_C/dV_{BE} = dJ_C/dV_{CE}$ because collector and base are connected, this measurement is different from 2-terminal conductance, because the base and collector currents are measured before they merge to the same potential, and therefore we are still characterizing three independent terminals. Hence, dJ_B/dV_{BE} is the base conductance, while dJ_C/dV_{BE} is the transconductance. To further clarify this point, we have measured the Gummel characteristics at different base-collector voltages V_{CB}, [29] as shown by the blue dots in figure 2. The effect of collector voltage on the collector current is much weaker than the effect of base-emitter voltage, and becomes negligible in the regime where the transistor gain is larger than unity. Hence, the contribution to dJ_C/dV_{BE} from ordinary collector conductance (e.g., dJ_C/dV_{CE}) is negligible compared to the transconductance contribution. There is no measurable effect of V_{CB} on base current, which shows that the mechanism responsible for the base current is decoupled from the base-collector junction.

The power dissipation in the transistor is calculated as emitter current times the base-emitter voltage. The original form is $I_B V_{BE} + I_C V_{CE}$. But because we bias collector at the same voltage as base, the formula reduces to $I_B V_{BE} + I_C V_{BE} = I_E V_{BE}$.

The inserts in the panels of Fig. 2 display the Gummel curves at room temperature. J is plotted on log-scale, showing the drift-diffusion scaling in $log(J)$ with $V/k_B T$. For V_{BE} (or V_{BC} in inverse mode) > 0.5V, the forward current gains ~ 400 are larger than the inverse current gains ~ 35, primarily due to the difference in collector and emitter doping levels. The reverse-active mode is used mainly here for characterization purposes.

At low temperatures, the drift-diffusion scaling clearly breaks down and discrete current steps emerge. Figs. 2**a**,**c**,**e** show that in the forward-mode, there exists a minimum base current density in the range $0.4 - 1\text{nA}/\mu\text{m}^2$, below which the current gain is less than unity. In contrast to the linear collector and base current at 300K, the curvature in the collector current at mK temperatures versus V_{BE} is positive below approximately 0.98V. As will be shown in Sec. III, the positive curvature is the signature of tunneling under the base potential barrier. In the inverse-mode data shown in Figs. 2**b**,**d**,**f**, the drift-diffusion scaling

also breaks down at low temperatures. However, in contrast to the forward-mode, devices 1 and 2 have current gain down to the lowest measured current density, as can be seen by the main panels in Figs. 2**b**,**d**. For example, at two base current densities of $J = 10^{-12}\mathrm{A}/\mu\mathrm{m}^2$ and $J = 10^{-11}\mathrm{A}/\mu\mathrm{m}^2$, the inverse current gains are 3 and 13 for device 1 and 16 and 17, for device 2, respectively.

With an increase in collector current density, the forward transistor current gain increases and becomes reasonably reproducible among the samples. For example, useful gains of 71, 56, and 80 in samples 1-3, respectively, are found at collector current density of $0.27\mu\mathrm{A}/\mu\mathrm{m}^2$. The power dissipation at that collector current is ≈ 0.1 μW, well below the cooling power of commercial dilution refrigerators (up to 400 μW). To prevent heating of the DR, we did not apply the maximum current drive. The measured base-emitter voltages averaged on the three samples at collector current densities of 1, 10, and 100 $\mathrm{pA}/\mu\mathrm{m}^2$ are 0.895 ± 0.01, 0.917 ± 0.01, and 0.923 ± 0.003V, respectively. As the base-emitter voltage increases at 70 mK, the current gain and transconductance increase quasi-exponentially, as shown in figure 3**a** and **b**.

The reproducibility between the samples demonstrates the viability of using these high performance (HP) SiGe HBTs at mK temperatures for building cryogenic integrated circuits, and suggests a common mechanism determining the collector current among the samples. The reproducibility with thermal cycling is remarkable. In sample 1, we find that the two lowest voltage steps are highly repeatable with thermal cycling between 300 K and DR-temperatures.

III. TUNNELING IN THE SIGE HBT AT DEEP CRYOGENIC TEMPERATURES

It is well known that quantum mechanical tunneling in SiGe HBTs contributes to parasitic base leakage current [31] and collector transport [23]. But the effect of tunneling in such cases is undesirable and related to traps present within the device. Here we present detailed simulations of the tunneling barrier, and compare ideal quantum mechanical tunneling under the barrier and measurement at mK temperatures. We find remarkable agreement between simulations and data in the forward-active mode of operation. Since carrier transfer in the *npn* SiGe HBT is responsible for the carrier depletion regions, the tunneling potential barrier

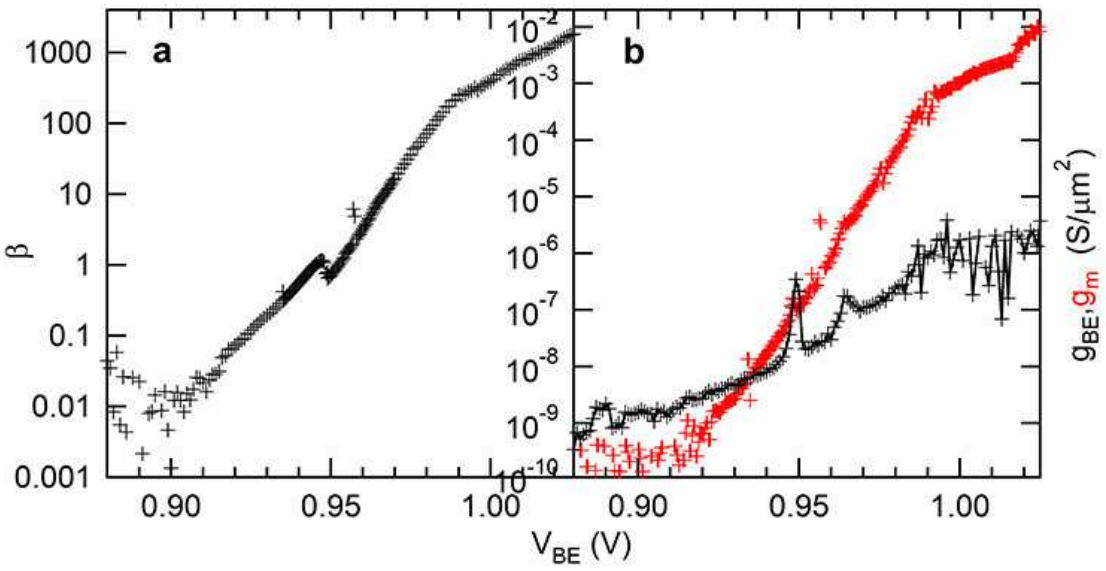

FIG. 3. Sample 1 at 70 mK temperature. **a**: Forward-mode current gain. **b**: Base differential conductance (black) and transconductance (red) per unit of area versus base-emitter voltage.

will be calculated self-consistently as a function of the base, emitter, and collector chemical potentials. The simulations were set up in the Synopsys Sentaurus TCAD suite using a realisitic SiGe HBT device structure with device doping profiles and geometries calibrated to match on-wafer DC and small-signal AC measurements of the GlobalFoundries 9HP platform. Simulations were performed using a hydrodynamic transport model for current densities with the parameter sets calibrated to 300 K measurement for the Phillips unified mobility model [32] and the Okuto-Crowell model for avalanche generation. [33] Simulated characteristics were performed in a common-base configuration by sweeping the emitter or collector voltage from 0 to 1.5 V for forward-mode and inverse-mode, respectively.

Our simulated barrier potentials are for 300 K. We expect the barriers to only modestly change in shape across temperature. Figs. 4**a**,**b** display the simulated band diagram of the measured SiGe HBTs at 0.8 V and 0.9 V base-emitter voltages, respectively. As in the experiment, the base and the collector are at the same chemical potential (i.e., grounded, so that the device is operated in forward-active mode). Also shown is the bottom of the conduction band at $V_{CB} = 0.5$ V at these two base-emitter voltages. The doping profiles and the Ge concentration are displayed in Fig. 4-**c**. The emitter is poly-Si which is heavily doped with As ($n = 10^{21}\text{cm}^{-3}$). The epitaxially grown and compositionally-graded $Si_{0.73}Ge_{0.27}$ base is aggressively doped with B (peak $p = 10^{20}\text{cm}^{-3}$). In Figure 4-**a**, the barrier height $\phi = 1.05$

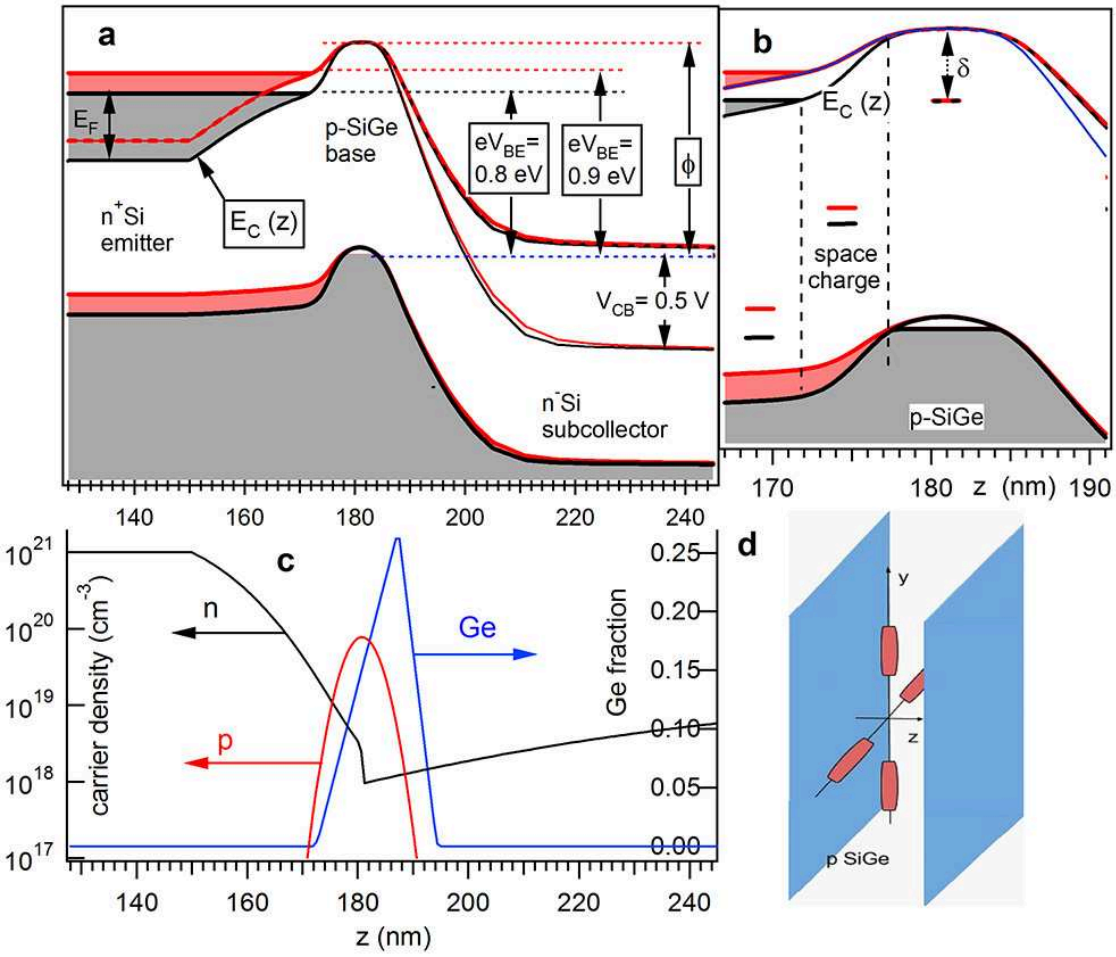

FIG. 4. SiGe-HBT composition: **a** and **b**: band diagram at V_{BE} of 0.8 V (black) and 0.9 V (red), and $V_{CB} = 0$ and 0.5 V. Trap levels in **b** are indicated by the short black and red horizontal lines, corresponding to V_{BE} of 0.8V and 0.9V, respectively. **c**: n and p are dopant densities and Ge grading versus position. **d**: Schematic of the four degenerate conduction band valleys in the transistor p-base.

V is defined as the difference between the maximum value of the bottom of the conduction band and the chemical potential at $V_{BE} = 0$V.

At the typical base-emitter voltage in the experiment of $V_{BE} = 0.9$ V, the simulated base-emitter depletion layer is approximately 6 nm thick, while the width of the entire tunneling barrier over the base is approximately 14 nm. In the idealized tunneling model near zero temperature, neither holes nor electrons are injected across the base-emitter junction. The holes do not tunnel from the base into the emitter, because the electron density of states in the emitter, at the energy range of the holes in the base, is zero. This can be seen in figure

4a, which shows that there are no electronic states in the emitter, in the energy interval between the Fermi level of the base and the top of the valence band in the base. Similarly, electrons do not tunnel from the emitter into the base, since there are no electronic states in the base at the required energy range (between eV and $eV - E_F$ in figure 4a). However, electrons can tunnel directly from the emitter to the collector, because the density of states in the collector is nonzero in the bias energy range $(eV, eV - E_F)$ of the emitter.

The small spatial extent of the barrier is critical for mK operation, which requires low power operation ($\sim \mu$W). The key to making a good amplifier at mK temperature is to make the electrons tunnel perfectly into the collector, at a rate higher than the rate of unwanted events. The thinner overall barrier increases the tunneling probability above that of these unwanted events. Trap assisted electron-hole capture in the base-emitter depletion layer, for example, can compete with ideal tunneling, thereby reducing the current gain and injection efficiency.

Now we can explain how amplification works in a SiGe-HBT operating at mK temperatures. An increase in base-emitter voltage by V increases the Fermi level in the emitter by eV, since the resistance of the emitter is negligibly small compared to the tunneling junction resistance. This reduces the charge and the electric field in the base-emitter depletion region, as usual in the *pn* junction. An equal and opposite reduction of the tunneling barrier potential is observed by the electrons in the emitter, which produces exponential increase in the tunneling current through the base, at the expense of a moderate base current required to increase the base voltage. The electrons emerging on the collector side of the barrier are rapidly moved into the neutral collector due to the strong electric field in the collector-base junction (about $7.5 \cdot 10^5$ V/m) and ballistic transport (due to the epitaxial collector quality and small doping).

It would be difficult to replicate this performance in a field effect transistor (FET). The operating principle of the FET is the electric field effect on carrier density in the conducting source-drain channel. The problem with the FETs is that the electric field is applied using capacitive coupling to the gate electrode. At this time, it is not technologically possible to make FETs with comparable channel length, the main problem being in the inability to make capacitors capable of reliably depleting carriers at such small length scale, [34] despite the impressive decrease in lateral feature size with scaling. This capacitance constraint is inherently absent in SiGe-HBTs, which can therefore operate on simple, yet predictable,

principles of quantum mechanics, as will be shown below.

The tunneling barrier in Fig. 4**a**,**b** expands over both the base and the space-charge regions (the space-charge region is the alternative word for the depletion region in the np-junction). Usually in the npn transistor at room temperature, one is mainly concerned with the potential difference about the space-charge region of the base-emitter junction. In that case the exponential dependence of collector current on base-emitter voltage is due to thermal activation over the tunneling barrier, so the collector current depends exponentially on the barrier height and not the barrier width. By contrast, at deep cryogenic temperatures, the collector current depends quasi-exponentially on both the barrier height and the extent of the barrier. In the conducting quasi-neutral base region, $E_C(z)$ (i.e., the conduction band energy at location z), is the barrier potential pinned to the chemical potential of the base. In the insulating space-charge region of the base-emitter junction, however, where the valence band is full and the conduction band is empty, $E_C(z)$ floats and will vary strongly with the base-emitter voltage. In this calculation, the drift diffusion terms are turned off.

The first calculations of the tunneling conductance in position-dependent barriers were carried out by Brinkman, Dynes, and Rowell (BDR). [35] For the tunneling current density we use the form derived by Floyd and Walmsley, [36]

$$J(V_{BE}) = \frac{4c\pi me}{h^3} \int_0^\infty F(E_F - E_z, T) P(E_z, V_{BE}) dE_z. \tag{1}$$

This equation will be valid only if $E_F < eV_{BE}$. In ideal BDR trapezoidal barriers $c = 1$, m is the free electron mass, $E_z = \hbar^2 k_z^2/2m$, $P(E_z, V)$ is the tunneling probability, and $F(x,T) = k_B T ln[1 + e^{x/k_B T}]$. At $T = 0$, $F(x,0) = x\theta(x)$ and the equation reduces to the equation 16 in Ref. [36]. Here, c accounts for band structure effects. We find $c = 4\sqrt{ab}$, where $a = 0.98$ and $b = 0.18$ are the ratios of the respective longitudinal and transverse effective electron masses, and the free electron mass m in the SiGe base. Prefactor 4 accounts for valley degeneracy. The SiGe base is pseudomorphically grown on the Si-100 surface of the n-type collector. The six-fold valley degeneracy of pure Si is broken due to compressive strain, and the bottom of the conduction band has four-fold valley degeneracy. That is, we suppose that the higher energy valleys will not contribute to the tunneling current. Fig. 4**d** displays the orientations of the four valleys with respect to the transistor heterostructure. Using the Wentzel-Kramer-Brillouin (WKB) approximation, we find

$$P(E_z, V_{BE}) = e^{-2\int \sqrt{\frac{2mb}{\hbar^2}(E_C(z) - eV_{BE} + E_F - E_z)} dz}, \tag{2}$$

where $E_C(z)$ is the bottom of the conduction band in the heterostructure obtained from the hydrodynamic TCAD simulations shown in Fig. 5**a**, the integral is taken over the region where the square-root is real, and a prefactor of order unity is not included. Figure 5**b** shows the calculated $J_C(V_{BE})$ curve for the transistor operating in the forward-active mode at $T = 0$. The current density exhibits positive curvature and an inflection point slightly above ϕ/e.

By comparing the $I - V$ curves in figures 5**b** and 2**a**,**c**, and **e**, we find that the measured and calculated collector current densities differ relative to each other in the range of plus/minus two orders of magnitude. Due to the exponential dependence of the tunneling probability on the details of the barrier potential, such an agreement is actually quite good. For a given collector current density, the difference between the measured and calculated base-emitter voltage varies in the range of 40 mV. The difference is only about five percent, which shows that the characteristic voltage for tunneling under the bottom of the conduction band accounts well for the measured voltage at which the collector current sharply increases.

According to the tunneling model at $T = 0$, we expect that the flux of electrons injected into the collector is distributed in a very narrow energy range just below eV_{BE}. This property is much different from familiar thermally-activated diffusion of minority carriers at room temperature, where electrons in the emitter need to be thermally activated above the barrier height, and therefore emerge in the collector with energy higher than eV_{BE}. In electron tunneling, there is a strong energy dependence of electron transmission probability through the barrier, so electrons with higher energy contribute exponentially more to collector current than those at lower energy. The exponential dependence therefore naturally selects injection of electrons at the highest energy accessible by the bias. The simulations find that the energy bandwidth of $[E_F - 10meV, E_F]$ in emitter conduction band contributes to 50% of collector current, for V_{BE} in the range in figure 5**b**.

We investigate this effect further by measuring the temperature dependence of collector current. If k_BT is much smaller than the transmission bandwidth of ≈ 10 meV, then the Fermi distribution in the emitter will not lead to additional broadening and the integral in Eq. 1 will be temperature independent. When k_BT approaches that bandwidth, then electrons in the high-energy tail of the Fermi distribution in the emitter will tunnel with higher probability, leading to an increase in J_C.

Figure 5**c** displays collector current density versus base-voltage measured in sample 1 and

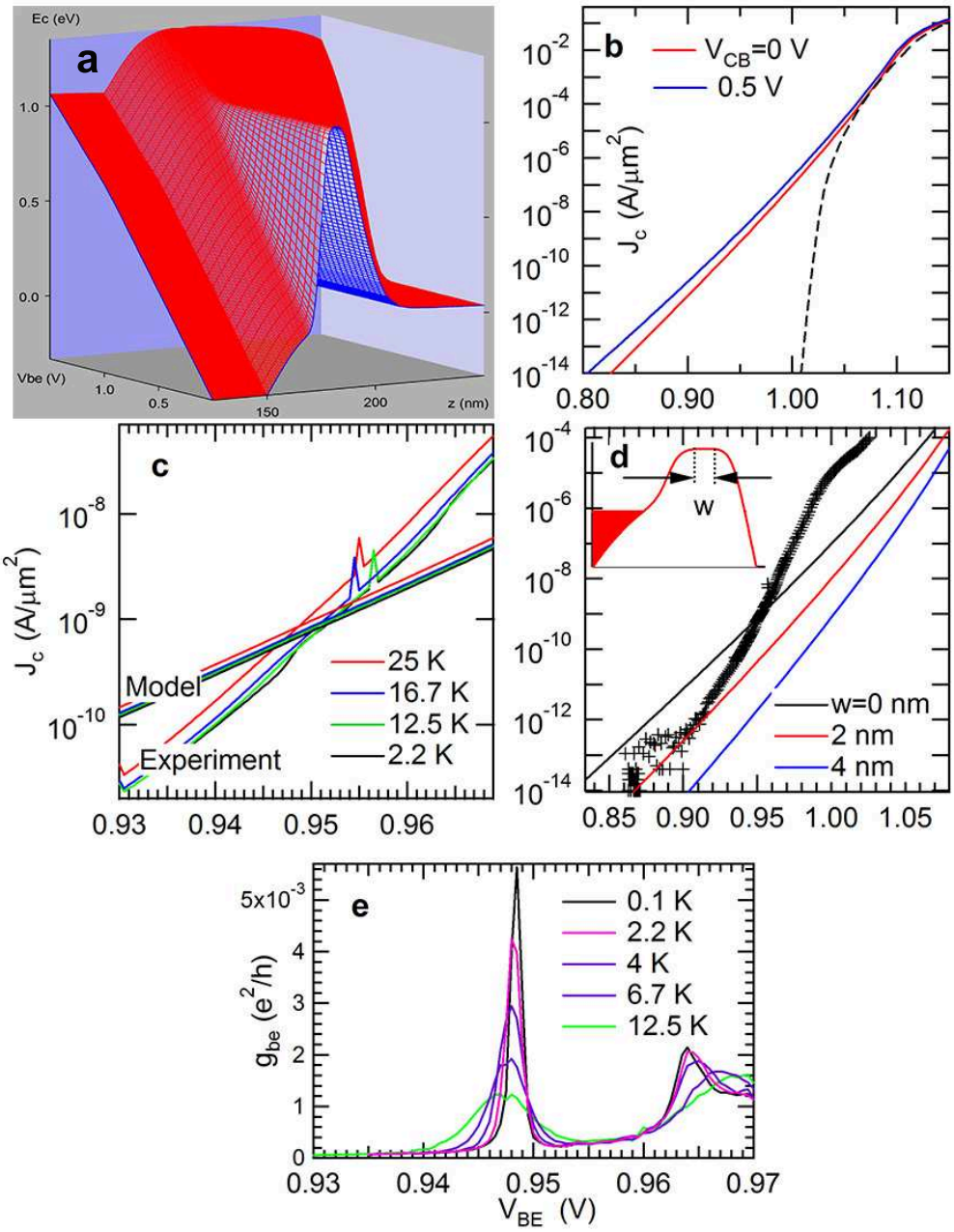

FIG. 5. **a**: Simulated bottom of the conduction band versus position and base-emitter voltage, in the forward-active mode. **b**: Simulated forward tunneling current density versus base-emitter voltage at two collector-base voltages and $T = 0$. Dashed line shows the corresponding inverse tunneling current density at zero emitter-base voltage. **c**: Forward collector current density measured in sample 1 and obtained by the simulation, respectively, versus V_{BE} and T. The glitches in the measurement are due to the range changes in parameter analyzer. **d**: The effect of barrier width w on forward collector current density versus V_{BE}, indicated by the lines. Symbols are data for sample 1 at 70 mK fridge temperature. The inset sketches the bottom of the conduction band versus position. **e**: Base-emitter conductance density in sample 1 measured at different temperatures.

that calculated using the idealized tunneling model. The effect of increasing temperature on $logJ_C(V_{BE})$ is well accounted for by a negative voltage shift. The temperature dependence saturates at approximately 16.7 K, below which the smooth IV curves, between the voltage steps, become invariant with temperature. Such invariance of transport properties of the transistor with temperature below some temperature may also be a signature of hot electron transport, [37] where drift-diffusion models fail because electron temperature stops changing. This poses a question how we know that there is quantum tunneling and not hot electron transport.

Figure 5**e** shows the base conductance measured simultaneously with the measurement in 5**c**. The conductance peaks are due to trap-assisted processes and have clearly a strong temperature dependence in the range down to $T \approx 1$ K. Thus, the saturation of the voltage shift in Fig. 5**c** at 16.7 K is not due to hot electron transport. The voltage shift is slightly larger in the data than simulation. This could be due to differences in barrier profiles between SiGe HBT samples and simulation. In particular, we find that decreasing the electric field by factor of 1.6 leads to an agreement with the measurement.

To illustrate the effect of the barrier profile, in Fig. 5-d we vary the width of the barrier and compare the simulated curves with the experimental data for sample 1. The wider barriers in this case are created by stitching a square potential barrier of width w at the barrier maximum, as shown by the inset of Fig. 5-d. While increasing the width of the barrier makes $\log J_C$ versus V_{BE} steeper, it also reduces the tunneling current. Further quantitative improvements of the model will require variation of doping and composition profiles, which is beyond the scope of this paper. However, qualitatively the collector current in these 9HP SiGe-HBT is within the range and has properties of idealized tunneling.

An important figure-of-merit in SiGe-HBT is the output resistance, dV_{CE}/dI_C. The effect of $V_{CB} = 0.5$ V on simulated tunneling current is shown by the blue line in Fig. 5**b**. The simulation reproduces the measurements shown in figure 2 quite well. The measured output resistance exceeds the simulated one by a factor of approximately two. Increasing the base-emitter voltage increases the output resistance. This effect can be explained as follows: consider a tunneling electron emerging from the barrier in the collector depletion region (Fig. 4). The higher the electron energy, the further away from the neutral collector the electrons will emerge, which reduces the dependence of the tunneling barrier profile on V_{CB} and leads to the higher output resistance (less dependence on collector voltage) at high V_{BE}.

In the reverse-active mode, the simulated emitter current versus base-collector voltage is shown by the dashed line in figure 5. The agreement between measured (Fig. 2**b**,**d**,**f**) and simulated emitter current is far worse than in the forward mode, especially at low bias. This may be somewhat surprising because the collector-base junction is epitaxially grown, while the emitter-base junction has poly-Si and therefore likely to have much higher defect density. The collector-base depletion region is much wider than the emitter-base depletion region, (e.g., 300 nm versus 6 nm). The large width of the barrier in the inverse mode reduces the tunneling rate by many orders of magnitude, and the current is therefore more susceptible to parasitic processes involving defects. This explains the prominence of current steps in the inverse mode compared to that in forward mode.

The step linewidths in the inverse-mode correspond to the electron temperature of approximately 250 mK, which shows again, following the same argument as in the forward-mode, that the transport at low bias voltage is not due to diffusion of hot electrons. [37] However, in contrast to the forward mode, the emitter transport at low bias is poorly described by the idealized tunneling. Instead, emitter current versus base-collector voltage has more voltage steps and higher fraction of the current represents the contribution from the traps, showing that trap assisted tunneling appears to be a more relevant electron transfer process than direct tunneling. The table below summarizes our present understanding of SiGe-HBT transport mechanisms at low temperature. Even though the reverse-forward mode at this time can exhibit current gain at lower base current density than in the forward-active mode, we believe that the forward mode has advantages. Industry is focused on improving the forward-active mode and does not emphasize the inverse mode. [38]

9HP SiGe HBT Properties	forward-active collector current	reverse-active emitter current
low bias, carriers not hot drift-diffusion negligible	not far from idealized tunneling	less understanding of quantum transfer processes, such as trap assisted tunneling, leakage through defects, etc. not desirable
high bias not possible to distinguish between contributions from diffusion of hot carriers and tunneling	high current gain	low current gain

IV. TRAP LEVELS IN SIGE HBT

The reproducibility of operation of advanced SiGe-HBTs at mK temperature demonstrated in Sec. II, and the agreement between the measured and modelled collector currents discussed in the previous section, lead to a natural question: If large scale integration of SiGe-HBTs are functional at mK temperatures (they clearly are), how should the circuit design be modified for optimized low temperature operation. To begin addressing these questions, learning about the effects of transistor self-heating at mK temperatures is of importance, since such heating can heat the device-under-test (DUT) through both the substrate and metal interconnects. Usually, the information about the transistor internal temperature is obtained by measuring the noise temperature of the amplifier, which is subject to impedance matching between the DUT and the transistor input. Here, information about transistor internal electron temperature is obtained directly by measuring the linewidth of discrete steps in the collector and base.

Discrete levels are involved in low temperature charge transport in semiconducting devices due to various impurities/traps/defects. [39] Figure 6 shows several possibilities of trap-assisted charge transport in SiGe-HBT. This picture implies that trap assisted transport is in general complicated. Each of the possible processes need to be evaluated step-by-step, to learn which one of those processes can be ruled out in the experiment, which is beyond the scope of this paper and will be published in future work. There are many possible sources

of impurities in SiGe HBTs: dopants, interfacial traps, carbon, oxygen, and other known defects in SiGe epitaxy. There are also many ways that the trap can be coupled to charge transport, including: tunneling, recombination, and capacitive coupling. Our measurements cannot distinguish between these trap locations and their couplings to transport. For example, sequential electron tunneling via the base trap and capacitive coupling between the emitter trap and broader collector tunneling will lead to a similar effects on collector current. These traps are generally undesirable because they can scatter the electrons away from ideal tunneling and therefore waste energy. As shown in the previous section, the collector current in 9HP SiGe HBT is already well-accounted for by the direct tunneling process, despite the presence of these traps. SiGe 9HP is a relatively new technology and the trap density is expected to improve over time due to process refinement, which should make the collector more ideal.

Despite their unwanted origin, the current steps observed in 9HP SiGe-HBT in Fig. 2 are very reproducible and with essentially no random telegraph noise, except for an occasional (but reproducible) glitch, likely caused by the instrument and wiring setup. In sample 1 we found that the two lowest steps with V_{BE} were reproducible even after thermal cycling to room temperature.

Gummel characteristics in Fig. 2 indicate that the steps broaden with V_{BE} and eventually become invisible. There is an observed trend that the steps in base current generally extend over wider voltage range than those in collector current. As an example, sample 2 displays a pronounced step in base-current at $V_{BE} = 0.95$ V, while the collector current versus V_{BE} is smooth and displays no step at that voltage (Fig. 2**a**). At 70 mK, there is a wide range of step widths in these SiGe-HBTs. While the overall trend is an increasing linewidth versus V_{BE}, there are significant fluctuations among different steps. Within the same sample, some steps at higher V_{BE} are narrower than some of those at lower V_{BE}. This means that the linewidth is influenced by factors other than just heating, since the latter can only increase with the applied V_{BE}.

A. Electron Temperature and Noise

Further analysis focuses on extracting the electron temperature T_e and noise linewidth from data. A reader primarily interested in applications may skip to section V.

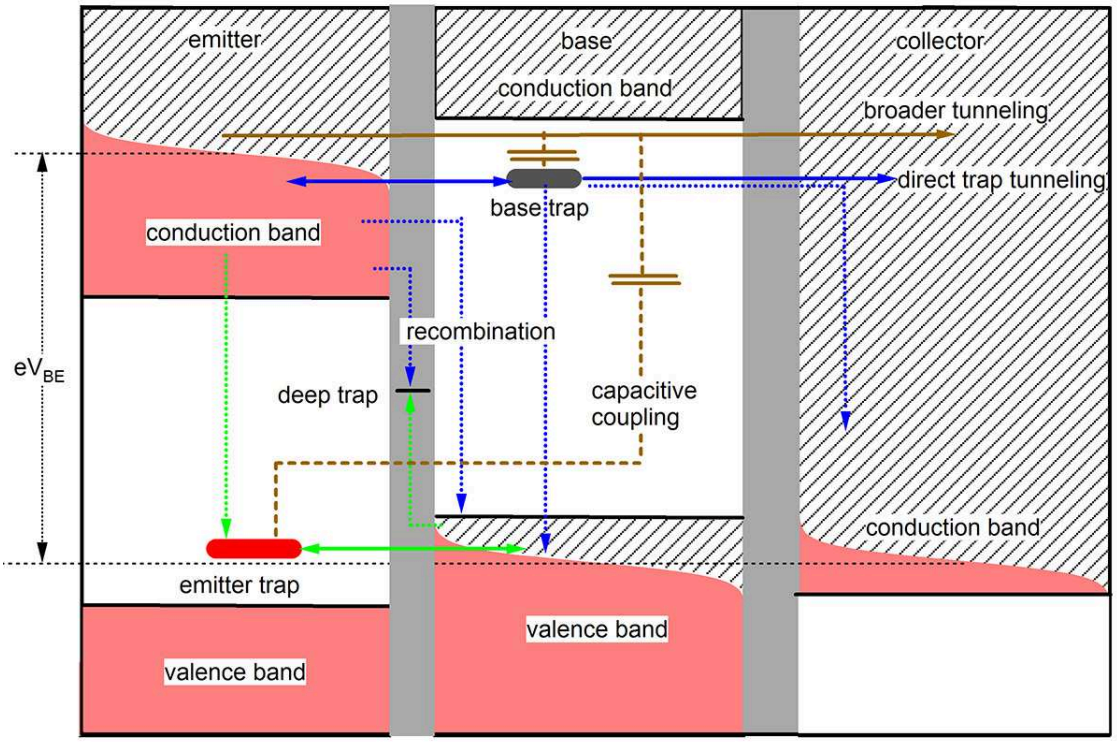

FIG. 6. Possible trap locations and their couplings to the transistor terminals by tunneling, recombination, and capacitively coupled transitions.

We select two particularly narrow steps in the base current which display negligibly weak step in the collector current, from Fig. 2. Having only two terminals simplifies the analysis. Figure 7**a** shows the lowest step (from now on step 1) in base current density versus base-emitter voltage in the forward-mode of sample 2 at different DR temperature. In this sample, another narrow step in base current (step 2) is found in the voltage range above the unity current gain regime and displayed in Fig. 7**b**. It can also be seen in the figure that the trap level does not display a corresponding step in the collector current. The maximum base-emitter conductance g_{BE} within steps 1 and 2 are $0.005e^2/h$ and $0.036e^2/h$, respectively. Fuechsle et al. [40] performed manipulations of single phosphorus atoms on the surface of silicon using a scanning tunneling microscope and fabricated a single-atom transistor with close to atomic resolution. They find in-plane tunneling conductance to be $0.05e^2/h$, for sequential transport via the phosphorous atom placed symmetrically between two electrodes separated by $\sim$ 19 nm. Shirkhorshidian et al. [41] studied the tunneling conductance of nearly defect-free silicon tunneling barriers. After implantation of approxi-

mately 10 antimony donors and annealing, they find the conductance per donor on the order of $0.1e^2/h$, for an extracted barrier width of $20-28$ nm. As discussed in section III the simulated base barrier width in the SiGe-HBT tunneling model is 14 nm, while the barrier width of 17 nm agrees better with the measurement. Thus, it is conceivable that step-2 could be due to tunneling into an unintentionally diffused donor impurity in the neutral base.

The width of step 1 at 70 mK is comparable to the voltage step 0.1 mV of the 4156C. However, if we compare the data at 70 mK and 100 mK, we find that the current densities at the following bias voltages: 0.8772 V, 0.8773 V, and 0.8774 V, do not fluctuate significantly between the two temperatures, despite the fact that the current density increases rapidly at those voltages. It logically follows that the energy resolution in our measurements is higher than the voltage step (multiplied by e) of the 4156C.

We define the voltage linewidth of the step as the full width at half maximum (FWHM_V) of the the corresponding peak in g_{BE} versus V_{BE}. FWHM_V is obtained by fitting the current step with V_{BE} to an appropriately scaled Fermi function, $f(V_{BE}) = J_p/[1 + \exp(e(V_p - V_{BE})/k_BT_L]$. The fit parameters are the step size J_p, the step voltage V_p, and parameter T_L, which is related to the voltage linewidth as $\mathrm{FWHM}_V = 3.52k_BT_L/e$. The lines between points in Fig. 7**a**,**b** are the best fits we found. We have added an offset to the conductance to account for the broader $J_b(V_{BE})$ dependence. We find $J_p = 0.014$ and 1.3 nA/μm^2 for steps 1 and 2. As V_{BE} sweeps through step 2, the power dissipation increases in the range $1.9-2.6$ nW.

Black stars and red squares in Fig. 7**b** display FWHM_V obtained from the fit, versus PPMS (ambient) temperature. For $T \geq 0.5$ K, the linewidth is approximately linear, with the best linear fits in that range are shown by the black and red lines (e.g., $\mathrm{FWHM}_V = k_B(3.48T + 0.197)/e$ and $k_B(3.52T + 1.69)/e$, for steps 1 and 2, respectively). These linear fits depend weakly on the profile function used for fitting. [42] The linear fit in step 2 does not extrapolate to zero, which is an indication that the broadening at 70mK ambient temperature is not due to self-heating.

In quantum dots, the step profile is usually a convolution of a Fermi distribution with a Lorentzian. [43] Let us assume that the charge transport through the trap is equivalent to electron tunneling in a quantum dot (e.g., a unit of charge is added to the trap from one terminal, followed by the removal of that charge unit), and this two step transfer process is

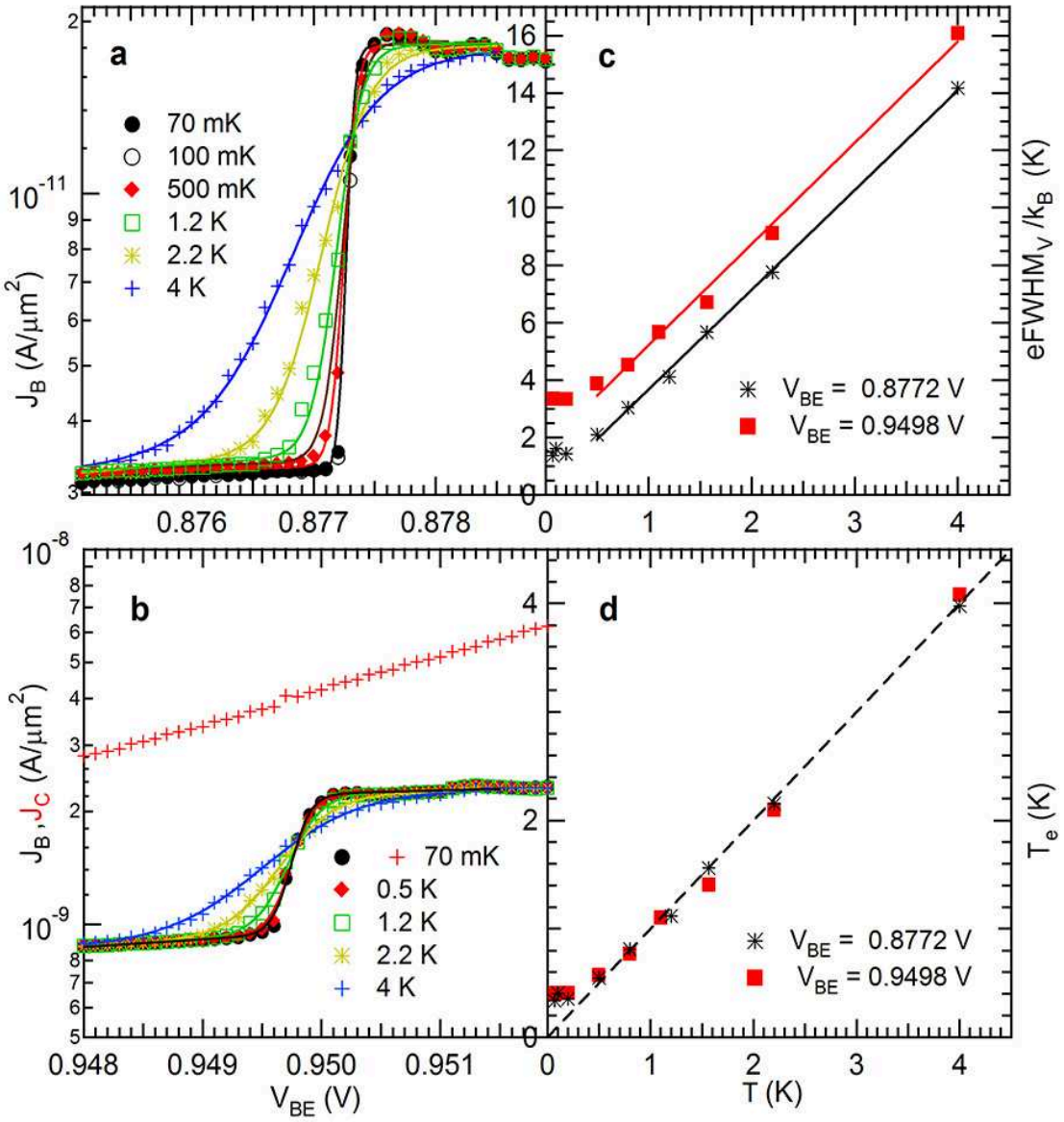

FIG. 7. Sample 2 at zero magnetic field. **a**: Discrete level profile versus DR-temperature, for the lowest step (step 1) in base current versus base-emitter voltage. **b**: Level lineshape for the base current step just above the onset of current gain (step 2), and the collector current density at 70 mK ambient temperature. In **a** and **b**, the symbols represent data and the lines are best fits to the Fermi function. **c**: Best fit full-width-at-half-maximum obtained from **a** and **b**, in units of temperature, versus ambient temperature, for step 1 (black stars) and step 2 (red squares). The lines are best linear fits. **d**: Electron temperature versus ambient temperature, showing that electrons do not cool below approximately 300 mK.

repeated sequentially, thereby leading to the base current. The FWHM of the Lorentzian, in units of energy, is $\gamma = \gamma_c + \gamma_d + \gamma_n$, [43] where $\gamma_c/\hbar$ and $\gamma_d/\hbar$ are the charge and discharge transfer rates between the trap and transistor terminals, and γ_n accounts for the coupling of the trap to a classical noise source. The noise source could be other electrons, traps, or shot noise. Classical means that the noise is symmetric in absorption and emission [43–45].

Straightforward calculations of the convolution find $\mathrm{FWHM}_E = 0.675\gamma + \sqrt{0.11\gamma^2 + (3.52k_BT_e)^2}$ (in units of energy), with error bar less than 1%, where T_e is the temperature of the Fermi distribution. If $k_BT_e \gg \gamma$, the convolution converges to a Fermi distribution with a $\mathrm{FWHM}_E = 0.675\gamma + 3.52k_BT_e$. T_e and T are not necessarily the same, due to the poor heat sinking of electrons at mK temperature (cooling power to the phonon bath is proportional to $T_e^5 - T^5$). At high T, $T_e \approx T$ since the cooling power increases rapidly with T_e.

By comparing the linear fits in FWHM_V at high ambient temperature to the linear fit in FWHM_E versus T_e, we have the lever arm. Somewhat unexpectedly, the voltage is converted to trap energy approximately as $E_t = eV_{BE}$. This means that the trap must be in the neutral regions of the transistor, since the chemical potentials in those regions are pinned to 0 or eV_{BE}, in the neutral base and emitter, respectively. For steps 1 and 2, the trap energies are 0.8773 and 0.9498 eV, and the linewidths are $\gamma = 0.025 \pm 0.015$ and 0.22 ± 0.04 meV. The proximity of E_t to the tunneling barrier height 1.05 eV shows that these are shallow traps. Shallow traps have been observed previously in single-shot readout circuits containing poly-Si, [2] but in that case they were hysteretic and not reproducible, unlike in this paper.

Now that γ is known, the electron temperature (T_e) in the transistor terminal can be obtained at any ambient temperature by a simple procedure, analogous to that used to account for Doppler broadening in atomic physics. Using the above expression for FWHM_E, we solve for T_e in terms of γ and FWHM_E, and display the result in Fig. 7**d**. $T_e(T)$ of the two steps have collapsed to the same curve, which is close to $T_e = T$ displayed by the dashed line. Thus, the effect of power dissipation at 2.2 nW on electron temperature is negligibly weak. The base electron temperature is $T_e = 0.38$ K.

B. Trap Levels in a Magnetic Field

Significant insights can be gained from the observed Zeeman splitting of the steps under an applied magnetic field. Fig. 8**a** displays base current density versus base-emitter voltage

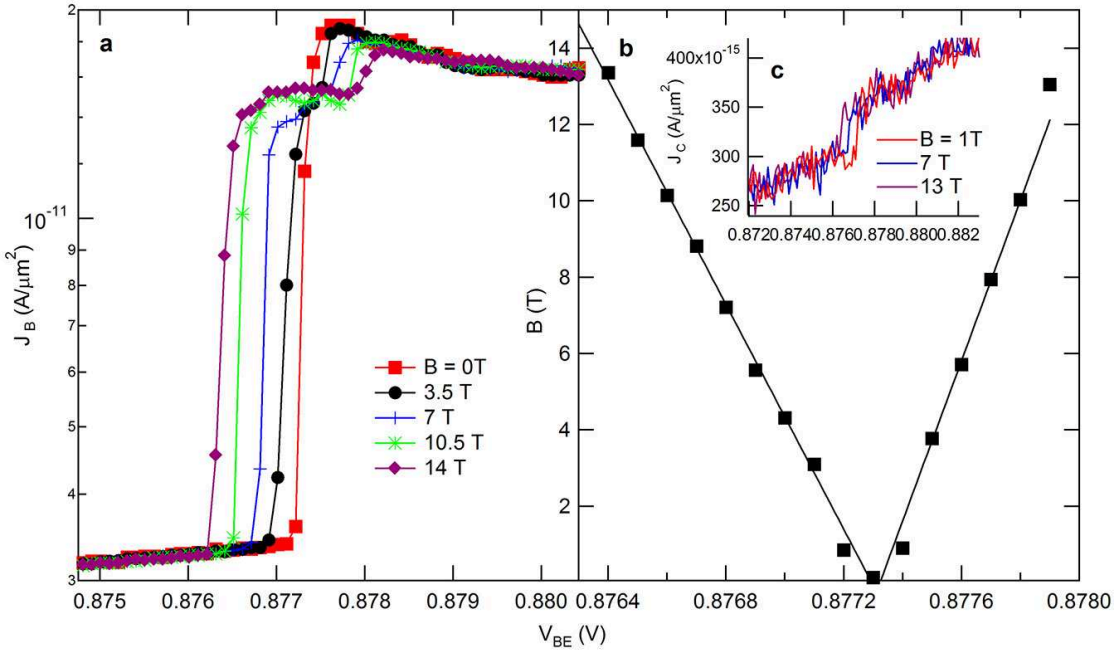

FIG. 8. Sample 2 at $T = 70$ mK. **a**: Level lineshape versus magnetic field, for the lowest step in base current versus base-emitter voltage. The symbols are data and the lines are guides to the eye. **b**: Full square symbols indicate V_{BE} at which the conductance has maximum at the given magnetic field. The lines are the best linear fits, leading to the g-factor in voltage splitting $g = e\Delta V_{BE}/\mu_B B = 2.00 \pm 0.03$. **c**: Nonzero current step in the collector current for the lowest step in base current versus V_{BE}.

in step 1, measured at different magnetic field applied perpendicular to the SiGe base. To obtain the splitting in voltage $\Delta V(B)$, we fit current versus magnetic field to the erf function, at each V_{BE} set by the 4156C (not shown). In this way, the error due to the finite voltage step of the 4156C is reduced. The center of the erf function provides the magnetic field at maximum differential conductance at given base-emitter voltage, and is displayed by filled squares in Fig. 8**b**. The erf function was used because, being a built in function in the software (wavemetrix), it is less likely to miss the fit due to poor choice of initial fit parameters. From the linear fits of step voltages versus magnetic field shown in the figure, we find $\Delta V = g\mu_B B/e$, where μ_B is the Bohr magneton and $g = 2.00 \pm 0.03$. Since $E_t \approx eV_p$, as shown in previous section, g is also the g-factor for energy splitting, in agreement with the g-factor in $Si_{0.73}Ge_{0.27}$ $g = 1.998 - 1.999$. [46] As shown in Fig. 8**c**, the level is displayed weakly in the collector current, with the step size of only $40\text{fA}/\mu\text{m}^2$.

The asymmetry of the amplitudes of the Zeeman split sub-levels can be used to extract all three linewidths γ_c, γ_d, and γ_n. In single-electron charge transfer via one nondegenerate quantum level, the step size in terms of the current (e.g., not current density) is approximately independent of γ_n and k_BT, and should be equal to $e\gamma_c\gamma_d/\hbar(\gamma_c+\gamma_d)$. [43] This is the current that flows through the lower energy Zeeman sublevel. If the level is two fold degenerate, however, then the current step should be $e2\gamma_c\gamma_d/\hbar(2\gamma_c+\gamma_d)$. The factor of two in front of γ_c is due to spin degeneracy. Coulomb repulsion between electrons prevents double occupancy, so γ_d is not multiplied by 2. This analysis is well established in the literature. [47]

Now we can determine all three linewidths of step 1 from the amplitude of Zeeman sublevels, and obtain $\gamma_c = 0.052$ μeV and $\gamma_d = 0.032$ μeV. Since $\gamma = 25 \pm 15$ μeV has large uncertainty (obtained in the previous section), we can only say that γ_n is smaller than or similar to 25 μeV. We repeated this analysis to step 2, and find the following parameters: $g = 1.95 \pm 0.05$, $\gamma_c = 2$ μeV, $\gamma_d = 4$ μeV, and $\gamma_n = 220 \pm 40$ μeV. So the broadening of step 2, which has a collector current two orders of magnitude higher relative to step 1, is almost entirely due to a noise source in the transistor.

We believe that the residual (temperature independent) broadening of the levels at low temperature is due the coupling between the trap level and shot-noise generated by the collector tunneling current. Or, in language of quantum computing, it is a form of back action noise from the collector current. In this back action, discrete charges transferred via the tunneling barrier dynamically couple to the trap level in the barrier, leading to energy exchange.

We constructed maps in the base and collector differential conductance with base-emitter voltage and magnetic field. An example is shown in Fig. 9, for sample 2. The color in Figs. 9**a** and **b** represents the logarithms of the base conductance density (dJ_B/dV_{BE}) and transconductance density (dJ_C/dV_{BE}), respectively. The base and the collector are shorted, as already stated. The discrete trap levels are displayed by the lines in the color maps. Between the base and the collector maps, 8 levels can be visually identified and labeled along the middle horizontal axis in Fig. 9 (level 1 corresponds to step 1 and level 8 corresponds to step 2).

Examination of the conductance maps reveals occasional coincidence between transconductance and base conductance levels. For example, in figure 9**b**, level 3 is visually present in both base-conductance and transconductance maps. However, some levels are found in

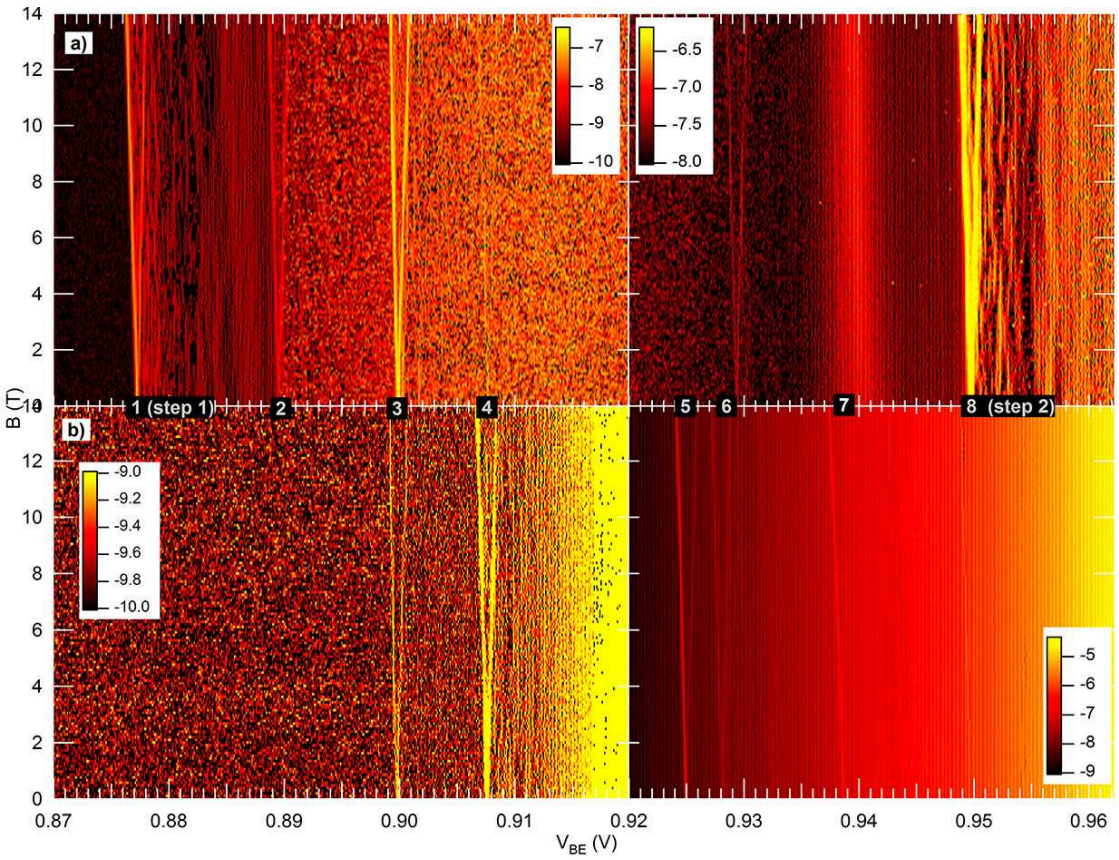

FIG. 9. Base conductance and transconductance map of SiGe HBT sample 2 at $T = 70$ mK. **a** and **b**: Color represents $\log dJ_B/dV_{BE}$ and $\log dJ_C/dV_{BE}$ with base-emitter voltage and magnetic field, respectively. Dark is lower value and orange is larger value. The sudden color shift at $V_{BE} = 0.92V$ is due to splitting the map to help with visibility of the colors.

one map only. Levels 1,2, and 8 are seen in conductance but not in transconductance. Level 5 is exhibited in transconductance but not base conductance. This distribution of trap levels between different terminals is likely an indication of random positions of the traps within the device.

V. DISCUSSION AND CONCLUSIONS

From a practical point of view, understanding the collector current and transconductance of SiGe-HBTs at deep cryogenic temperatures in terms of ideal quantum mechanical tunneling through a well-simulated barrier, is a critical step towards optimizing SiGe-HBTs for mK temperature operation and hence useful circuits. Because the current gain depends strongly

on the base current, the circuit designer needs to take into account the output non-linearity when the output swing increases. If the nonlinearity is still an issue, they should characterize the circuit before actual use and determine the gain versus base current characteristics and limit the circuit operation to regions where the nonlinearity is not an issue. The steps in collector and base current will not affect circuit design, since the transistor will either be used in the bias voltage regime where the steps are not resolved or the traps will be removed with technological improvement. The designer also needs to take into account that the power dissipation must be kept low, to not compete with the cooling power of DR (up to 400 μW at 100 mK) and to not heat the DUT. Thus, peak transistor performance may not be achievable at mK temperatures unless more cooling capacity is available.

One potential issue with these SiGe-HBTs is that the current gain becomes smaller than unity at low base current due to parasitic base leakage (recombination). Fundamentally, the solution would be to reduce the base current density relative to the collector current density and thus increase the input impedance. This will be difficult to accomplish because it is physically impossible to eliminate the recombination of minority carriers in the base while maintaining the tunneling current. The recombination rate in the base is logically proportional to the probability to find an electron in the base, and this probability cannot be zero if there is to be tunneling into the collector. This competition between tunneling and recombination is indicated by the green circle junction in figure 6. Reducing the base width will favor tunneling to recombination. While we anticipate only modest improvement in unity gain base current density, this is not seen as a major issue, as will be discussed next.

Degenerately-doped SiGe HBTs can potentially be used to construct viable amplifiers at mK temperatures, exhibiting low power dissipation and high transconductance. SiGe HBTs are attractive for amplifiers at mK temperatures due to the low cost of silicon technology, availability from foundries, and integrability with silicon electronics (i.e., high levels of integration), including silicon quantum electronics. [48] The suppression of the current gain at very low base-currents could potentially be problematic for amplification of currents in high resistance mesoscopic samples, like nanoparticles or single molecules, or in qubit readouts. The unity gain base current can be reduced further by reducing the emitter area. However, a useful current gain in these studied devices is found at base current of a few nA, which is sufficient for many experiments in mesoscopic physics, as well as for basic circuit building. The next steps will be to investigate the variations among various SiGe HBT scaling

generations, and their advantages and disadvantages relative to other amplifiers that can be constructed (e.g., HEMTs), as well as the fabrication of basic circuits capable of operating at mK temperatures.

It is demonstrated in this paper that the collector current in these advanced silicon germanium transistors is mostly due to ideal quantum mechanical tunneling of electrons under the potential barrier extending through the entire base. An increase in base voltage creates an equal but opposite decrease in barrier potential in the emitter-collector channel, seen by the electrons in the emitter. Due to exponential dependence of tunneling probability on barrier height, a large tunneling current is switched on by a moderate amount of current required to increase the base voltage. This remarkable simplicity of amplification in advanced SiGe-HBTs at deep cryogenic temperatures stands in contrast with more complex amplification in a field effect transistor, which is based on electron mobility and capacitive coupling to the gate. The reason why these advanced SiGe-HBTs operate so well is that the base is inherently extremely thin, and as a result the tunneling probability is sufficiently large to become the dominant electron transfer process. Realization of such an amplifier in a robust and manufacturable silicon-germanium transistor, and the ability to simulate the tunneling barrier potential and further optimize it, is a critical step toward manufacturing complex but useful circuits operating on basic principles of quantum mechanics.

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