Bandlike Transport in Ferroelectric-Based Organic Field-Effect Transistors

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Band-like transport in ferroelectric-based organic field-effect transistors

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Abstract

The dielectric constant of polymer ferroelectric dielectrics may be tuned by changing the temperature, offering a platform for monitoring changes in interfacial transport with the polarization strength in organic field-effect transistors (FETs). Temperature dependent transport studies of FETs have been carried out from a solution-processed organic semiconductor, 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene), using both ferroelectric and non-ferroelectric gate insulators. Non-ferroelectric dielectric based TIPS-pentacene FETs show a clear activated transport in contrast to the ferroelectric dielectric polymer, poly(vinylidene fluoride-trifluoroethylene) (PVDF-TrFE), where a negative temperature coefficient of the mobility is observed in the ferroelectric temperature range. The current-voltage (I-V) characteristics from TIPS-pentacene diodes signal a space-charge-limited conduction (SCLC) for a discrete set of trap levels, suggesting that charge injection and transport occurs through regions of ordering in the semiconductor. The carrier mobility extracted from temperature-dependent I-V characteristics from the trap-free SCLC region shows a negative coefficient beyond 200 K, similar to the trend observed in FETs with the ferroelectric dielectric. At moderate temperatures, the polarization fluctuation dominant transport inherent to a ferroelectric dielectric in conjunction with the nature of traps results in an effective de-trapping of the shallow trap states into more mobile states in TIPS-pentacene.

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I. INTRODUCTION

The general mechanism of transport in organic field-effect transistors (FETs) constituting molecular or polymeric semiconductors has been mainly addressed within the framework of hopping between disordered-localized states. The process, however, is more complex since there are several competing factors that result in extended band states in organic semiconductors, and factors that result in localized states such as the off-diagonal thermal disorder [1]. Electronic polarization effects — short-range and long-range lattice fluctuations — play an inherent role in FET transport. The polaronic nature of the charge carriers is heavily masked by disorder effects; both local and non-local electron-phonon coupling are required for a comprehensive theoretical model [2]. In single-crystal organic FETs such as rubrene, the disorder is significantly reduced, enabling the realization of intrinsic polaronic transport including the observation of the Hall effect in the accumulation layer [3]. The Hall voltage is a sensitive probe that measures the extent of delocalized adiabatic transport. The presence of normal Hall effect in organic FETs is therefore a signature that the surface charge is similar to a two-dimensional hole or electron-gas system rather than a hopping of carriers [4].

There have been several recent works that show band-like transport, characterized by negative coefficient of the charge carrier mobility (μ) with respect to temperature (T) ($d\mu/dT < 0$), in solution-processable small molecule and polymer based FETs. In 6, 13-bis (triisopropylsilylethynyl)-pentacene (TIPS-pentacene), a negative coefficient of the carrier mobility at high electric fields was attributed to localized transport limited by thermal lattice fluctuation [5]. In a few acene based solution processable small molecule FETs, charge delocalization induced by the dynamic disorder as a function of temperature has been probed by charge modulation spectroscopy, shedding light into the nature of shallow traps [6]. By incorporating large thermal lattice fluctuations with weak van der Waals intermolecular bonding, theoretical models have explained the band-like motion observed at high temperatures from highly conducting organic semiconductors [1]. In such materials, the carriers diffuse incoherently in the presence of the large thermal fluctuations, resulting in a weakly metallic behavior. Band-like transport in TIPS-pentacene FETs has also been observed by time-resolved optical second-harmonic generation imaging [7].

In high mobility donor-acceptor-type diketopyrrolopyrrole (DPP) conjugated polymers, a

low degree of disorder and a negative coefficient of the carrier mobility (with respect to temperature) were found to be consistent with Hall voltage measurements [8]. A benzotriazole based DPP system exhibits a band-like temperature dependence of the FET mobility when transport is preferentially along the polymer chain alignment direction [9]. In benzothiadiazole copolymer based FETs, charge transport properties have been shown to approach disorder-free limits where all molecular sites are accessible [10].

The low degree of disorder, a much wanted feature in polymeric semiconductors, is a combination of the coplanar structure supporting wavefunction delocalization and other macroscopic attributes of the material. A common feature for $d\mu/dT < 0$ to occur beyond a certain temperature, as seen across a variety of organic semiconductors, is that the FET carrier mobility should be larger than $\mu_{min} = er^2/2\hbar$, where r is the intermolecular distance, e is electronic charge, and $\hbar$ is the Planck's constant [11]. Typically, this condition translates to FET mobilities being greater than 1-2 cm^2/Vs, ensuring that the energy bandwidth is larger than the energy change involved in scattering. Recently, ac Hall effect measurements have shed light into the coexistence of both band-like and hopping charge carriers in the accumulation region of organic FETs. Due to this mixed transport regime, even when FET carrier mobilities are less than 1 cm^2/Vs, a Hall voltage is measurable [12, 13]. We later show that the coexistence of band-like and hopping carriers may be attributed to the nature of the shallow traps - discrete traps or a distribution of trap energies.

At this point it may be prudent to point out that band-like transport in molecular semiconductors, which mainly occurs in narrow bands, is somewhat different from true band transport, where the latter occurs through extended states in perfect crystals. In pure organic crystals such as naphthalene, band transport for electrons was observed below 150 K [14]. Subsequently first-principles calculations involving inter- and intra-molecular vibrations and electron-phonon coupling constants (both local and non-local) have shed light into the band to hopping transition in naphthalene as a function of temperature [15]. This transition can be understood on the basis of a localization of charge carriers in the absence of any thermal disorder. Furthermore, at the transition where the charge may be more delocalized, raising the temperature destroys the translational symmetry and reduces the charge transport efficiency and thus its mobility [16]. The apparent band-like transport observed as $d\mu/dT < 0$ in organic/polymeric FETs may be mediated by extrinsic mechanisms. As we see in this work, depending on the nature of the dielectric used, a negative or a positive

coefficient of μ with respect to temperature is observed in TIPS-pentacene FETs, and this behavior is further correlated to the nature of the shallow traps.

The semiconductor-dielectric interface plays a major role in dictating the transport properties in FETs. One aspect in FET transport arises from polarization fluctuations, especially when polar dielectrics are used. The dynamic coupling of charge carriers to the electronic polarization at the semiconductor-dielectric interface arises mainly from two effects: the image force due to the polarization discontinuity at the interface and the Coulomb interaction of the charge carriers with the surface phonons of the dielectric [17, 18]. It has been shown that Fröhlich surface polarons are formed if the gate dielectric is sufficiently polar in molecular systems [19]. The Fröhlich polarons arise due to a long-range interaction between the charge carriers and the longitudinal optical phonons [20]. These interactions result in a renormalization of the transfer integral and decrease the charge carrier mobility.

Ferroelectric dielectrics, permitting access to nearly an order of magnitude range of dielectric constants with temperature as the tuning parameter, offer a neat platform to monitor the changes in interfacial transport in organic FETs as the polarization strength is tuned. Temperature-dependent transport studies from pentacene FETs using the ferroelectric copolymer poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) showed a suppressed hole mobility in the ferroelectric phase of the dielectric [21]; similar characteristics were also observed in poly hexyl-thiophene (P3HT)/PVDF-TrFE FETs [22].

In this work we explore the influence of both ferroelectric and non-ferroelectric dielectrics on the transport mechanism in TIPS-pentacene FETs using top-gate and bottom-gate architectures. Unlike non-ferroelectric dielectrics, the temperature dependent mobility when using PVDF-TrFE shows a negative coefficient beyond 200 K, similar to a weakly metallic behavior. Interestingly, the current-voltage characteristics from TIPS-pentacene diodes signal a space-charge-limited conduction (SCLC) for a discrete set of trap levels, suggesting that charge injection and transport occurs through regions of ordering in the semiconductor. The carrier mobility extracted from temperature-dependent current-voltage characteristics from the trap-free SCLC region shows a negative coefficient beyond 200 K, similar to the trend observed in FETs with the ferroelectric dielectric.

II. EXPERIMENTAL DETAILS

A. Materials

6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) was procured from Sigma Aldrich, Inc. and used without any purification. Pentacene was procured from Tokyo Chemical Industry. The dielectric, poly[(vinylidenefluoride-co trifluoroethylene] (PVDF-TrFE) (75/25) was obtained from Measurement Specialties, Inc., USA. Poly-4-vinyl phenol (PVP) with average molecular weight (Mw) 25000 g/mol, propylene glycol monomethyl ether acetate (PGMEA) with Mw 132.16 g/mol, and crosslinking agent poly(melamine-coformaldehyde)methylated 84 %solution in 1 butane (PMMF) were procured from Sigma Aldrich, Inc. The solvents N,N-Dimethylformamide (DMF) and anhydrous toluene were procured from Sigma Aldrich, Inc. CYTOP (CTL-809M) was bought from Asahi Glass Co. Ltd. Japan. Glass substrates and SiO2 on Si^{++} wafers were obtained from Fisher Scientific and Silicon Quest International, respectively.

B. Device fabrication

Bottom-gate top contact and top-gate bottom contact FETs were fabricated by evaporating 60 nm aluminum as gate using a shadow mask. The PVDF-TrFE dielectric layer on glass substrates were obtained as described in a prior work [21]. The ferroelectric phase occurs in the all-trans or the β-phase of the co-polymer. Unlike PVDF, the co-polymer, PVDF-TrFE has the advantage of being ferroelectric directly after solution processing of the film [23]. Annealing the film at 135 °C further enhances the β-phase of the co-polymer. X-ray diffraction and Raman scattering from our annealed PVDF-TrFE films confirmed the presence of the β phase. The PVP layer on Al coated glass slides were printed using inkjet printing (Diamtix Materials Printer 2831). A 5 wt% solution of PVP in PGMEA with 2 wt% of crosslinking agent PMMF was heated at 60 °C for 1 hour before printing. This solution was filtered through 0.45 μm PTFE filter. Substrate temperature of 60 °C and 50 μm drop spacing improved the jetting of PVP and minimized the number of pinholes in the film. The PVP layer was printed twice to improve the capacitance of the device. After printing, the substrates were moved to a nitrogen environment and annealed at 180 °C for 1 hour.

TIPS-pentacene was dissolved in anhydrous toluene and stirred on a hot plate with a magnetic stirrer at 60 °C. The TIPS-pentacene film was obtained through slow crystallization growth in a solvent-saturated atmosphere. The orientation of the crystal axes was achieved by positioning the substrate inside a Petri dish at a 2 ° angle with respect to the horizontal. Substrates were placed inside the Petri dish in a manner such that the length of the channel was parallel to the receding direction of the drying solution. Drop casting was carried out using a pipette with the substrate kept at 50 °C ; the lid was put back immediately afterwards to trap the solvent vapor and create a vapor saturated condition inside the Petri dish. Pentacene films (60 nm) were obtained via thermal evaporation process (0.3Å/s, 10^{-5} mbar) for fabrication of diodes. All organic semiconducting films were followed by 50 nm thermally evaporated gold electrodes. For top-gate bottom contact FETs, CYTOP was spin-coated on top of TIPS-pentacene which was followed by 60 nm aluminum as top gate. The dielectric film thicknesses were inferred from capacitance measurements of metal insulating semiconducting (MIS) devices (in the accumulation region) and further confirmed with a reflectometer. The thickness of the dielectric layers are listed in Table I.

C. Device characterization

Room temperature DC electrical characterizations were performed using two source-meters, Keithley 2400 and Keithley 236, using a customized LabVIEW program. For temperature-dependent electrical measurements, a dual source-meter Keithley 2612B was used. The FETs were kept inside a closed-cycle helium cryostat (APD Cryogenics) where the temperature may be varied from 11 K to 480 K. The temperature was measured using a Lakeshore 330 temperature controller. The temperature dependence of both TIPS-pentacene and pentacene diodes were also measured with the APD cryostat.

The capacitance measurements from MIS diodes were carried out with an HP 4284A precision LCR meter. During the measurement, a DC voltage is applied to the capacitor with a small AC voltage signal superimposed over the DC signal. Capacitance is recorded as the DC bias is swept. The magnitude of the AC signal was 200 mV and the frequency of the signal was 5 kHz for all measurements. The DC signal was swept both from positive to negative bias and vice versa.

TABLE I. Thickness of the dielectric layers and average carrier mobilities from TIPS-pentacene FETs with different dielectrics at room temperature.

	PVDF-TrFE	SiO_2	PVP	CYTOP
Dielectric thickness (nm)	430	200	120	180
Average mobility (cm^2/Vs)	0.003±0.001	0.073±0.014	0.13 ±0.010	0.17 ±0.02

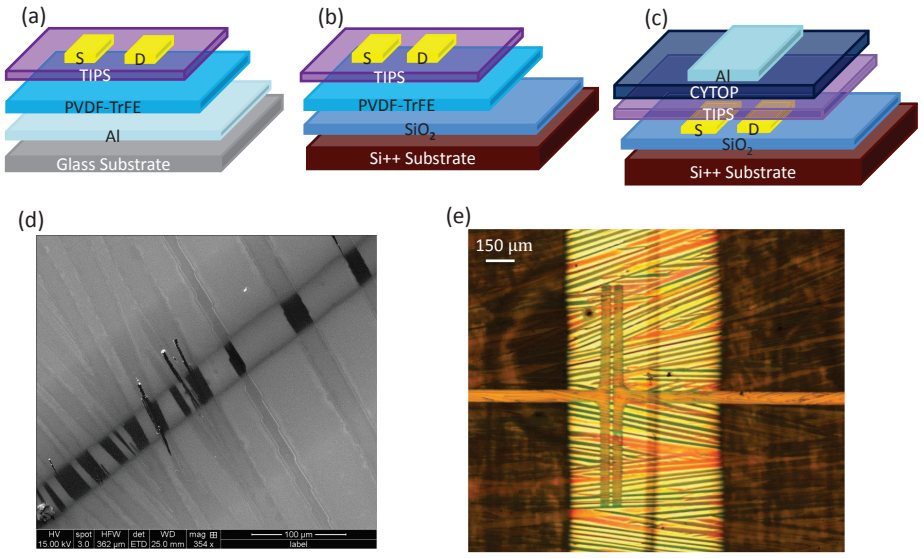

FIG. 1. FET device structures. (a) Bottom-gate, top contact with PVDF-TrFE; (b) bilayer bottom-gate with top contact; and (c) dual FET with SiO_2 as the bottom-gate and CYTOP as the top-gate. (d) TIPS-pentacene on SiO_2 (SEM image). (e) TIPS-pentacene on PVDF-TrFE (optical image).

III. RESULTS AND DISCUSSIONS

Fig. 1 shows a schematic of FET architectures used in this work. All PVDF-TrFE and Poly-4-vinyl phenol (PVP) based FETs were fabricated as bottom-gate structures with aluminum as the gate electrode. The SiO_2 based FETs were fabricated as bottom-gate/bottom contact structures. Bilayer SiO_2/PVDF-TrFE dielectrics (Fig. 1(b)) were also used. For the CYTOP dielectric, TIPS-pentacene was grown on SiO_2/Si^{++} substrates as shown in Fig. 1(c), which had the advantage that the same TIPS-pentacene film could be probed using two different dielectrics. This was also done for another batch of FETs with PVDF-TrFE as

the bottom-gate (with bottom contacts) and CYTOP as the top-gate. Fig. 1(e) shows an optical image of TIPS-pentacene on the PVDF-TrFE layer. The crystalline grains grow more or less parallel to the S/D contacts in the direction of charge flow. The parallel growth of TIPS-pentacene is further seen in a scanning electron microscope (SEM) image (Fig. 1(d)).

A. FET characteristics

1. Room temperature FET characteristics

Typical current-voltage output and transfer characteristics of TIPS-pentacene FETs on SiO_2 and PVDF-TrFE dielectric layers are shown in Fig. 2(a-d). The FET properties were found to be strongly dependent upon the nature of the dielectric used; SiO_2 based FETs show a better performance than PVDF-TrFE based FETs. This is not surprising since PVDF based dielectrics have a higher surface roughness [24] and are more conducting compared with other polymer and oxide dielectrics, resulting in a lower ON/OFF ratio. There have been several strategies for improving the surface roughness and morphology of PVDF based films by adding thin insulting layers, micro-patterning, and optimization of annealing conditions [25–27].

The FET mobility was obtained from the saturation regime by using $\mu = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_G}\right)^2$, where C_i is the dielectric capacitance, W is the channel width, L is the channel length, V_G is the gate voltage, I_{DS} is the drain current, and μ is the field-effect mobility. For the transfer characteristics, the gate voltage was swept up to V_{DS}, which was selected in the saturation regime. By applying a linear fit to the saturation region the hole mobilities were extracted for all sets of FETs. Several devices were measured and the results shown in Fig. 2 are typical from a set of 5-6 devices. The ON/OFF ratios were $> 10^5$ for the SiO_2/TIPS-pentacene FETs and slightly lower for other dielectric based devices. Some of the best performing devices resulted in $\mu = 0.2$ cm^2/Vs for CYTOP/TIPS-pentacene and 0.3 cm^2/Vs for the PVP dielectric. The average values of FET mobilities at room temperature with their standard deviation for the different dielectrics are shown in Table I. The average values of the carrier mobilities at 300 K as a function of the dielectric constant are found in Fig. S1 [28]. There is a clear trend of reduced mobility with increase in the dielectric constant of the insulating layer. It is not surprising that although PVP and SiO_2 have

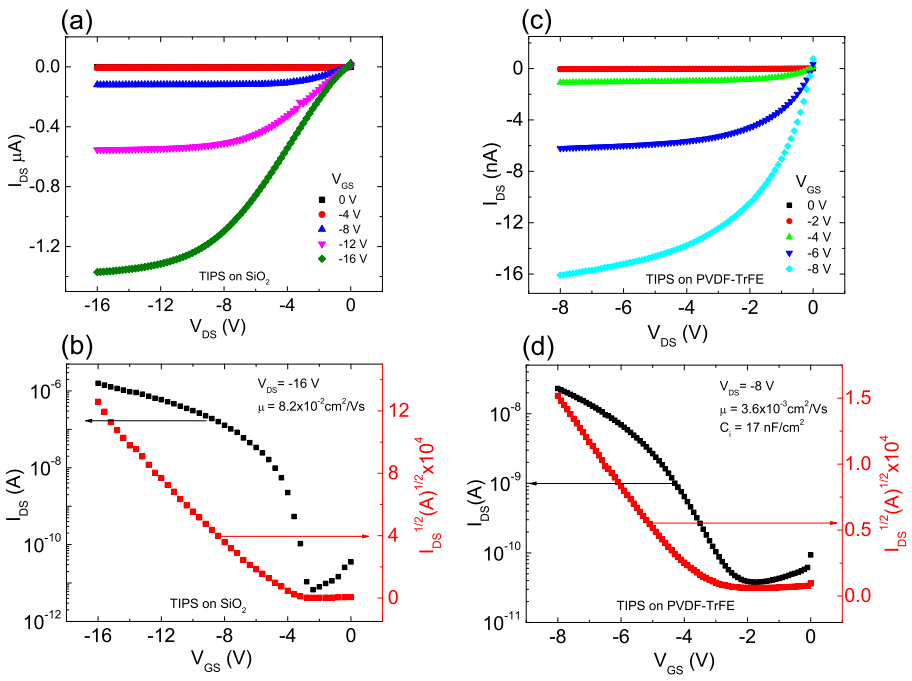

FIG. 2. (a) and (b) Output and transfer characteristics of TIPS-pentacene on SiO_2 FET. (c) and (d) Output and transfer characteristics of TIPS-pentacene on PVDF-TrFE FET.

similar dielectric constants, FETs with SiO_2 as the dielectric layer show a lower carrier mobility. Oxide dielectrics are known to trap more charges at the interface compared to polymer dielectrics.

2. Temperature dependent FET characteristics

The temperature dependent FET characteristics of TIPS-pentacene were measured from several devices with different dielectrics. We first focus on the difference between PVDF-TrFE and SiO_2. Since TIPS-pentacene films have been known to develop cracks above 340 K [29], our measurements were performed till $\sim$ 320 K. This adds a constraint for the ferroelectric dielectric as the FET measurements could not be performed till the ferroelectric paraelectric transition, which occurs at $\sim$ 390 K in PVDF-TrFE [22, 30]. The transconductance curves at different temperatures are plotted for TIPS-pentacene FETs on SiO_2 and PVDF-TrFE in Figs. 3(a) and (c), respectively. In TIPS-pentacene/SiO_2, the slope of the transconductance curve is seen to increase with temperature whereas in the TIPS-pentacene/PVDF-TrFE FET, the slope of the transconductance decreases beyond $\sim$ 240 K,

(see inset in Fig. 3(c)). The extracted mobilities shown in Fig. 3(d) clearly show this trend. The FET mobilities for the SiO_2 device are plotted in Fig. 3(b); the trapped charge density (N_{trap}) obtained from the subthreshold swing of the transfer characteristics as a function of temperature is shown in the inset. We point out that other analytical methods yield more accurate values of trap densities [31]. With PVDF-TrFE, however, N_{trap} is seen to be discontinuous at the transition temperature, which was shown in P3HT [22] and pentacene based FETs [21].

The channel lengths of our FETs were 50 - 100 μm. As observed in many works the contact resistance for such long channel devices is negligible compared to the channel resistance [8, 32]. Usually the transistor performance is contact limited for channel lengths $\leq$ 10 μm [33]. For SiO_2, PVP, and CYTOP, the contact resistances of TIPS-pentacene FETs were a few orders of magnitude smaller than the channel resistance. For the PVDF-TrFE devices the contact resistance was roughly two orders of magnitude smaller than the channel resistance. The slightly higher contact resistance with PVDF-TrFE has been attributed to the polarization fluctuation at the semiconductor/ferroelectric interface, which broadens the trap charge distribution in the contact region of the semiconductor [34]. Furthermore, the contact resistance does not change much in the 100 K - 300 K range [35], the temperature range used in this work. Given the long channel length of our devices and some of the established work showing the almost temperature independence of Au contacts, the contact resistance does not significantly affect the transport measurements.

The leakage (gate) current was three orders of magnitude smaller than the drain current for PVDF-TrFE and PVP based FETs and did not change very much with temperature [28], which ensures that the extracted carrier mobilities at different temperatures, especially for PVDF-TrFE, are not affected by the gate current. The gate current for CYTOP and SiO_2 is slightly higher than in PVP and PVDF-TrFE although the ratio of the drain to gate current even for these FETs is comparable to other works [36].

Variable-temperature studies of organic FETs typically reveal thermally activated transport where the carrier mobility is attributed to an energetic disorder described in terms of thermally assisted hopping. This can be fitted with an Arrhenius type behavior with activation energy (Δ), in the order of tens to hundreds of millielectronvolts, arising from polaron relaxation or from models based on multiple trap levels [37–39]. In such a mechanism, the carrier mobility is given by $\mu = \mu_0 \exp(\frac{-\Delta}{k_B T})$, where μ_0 is the mobility in the absence of any

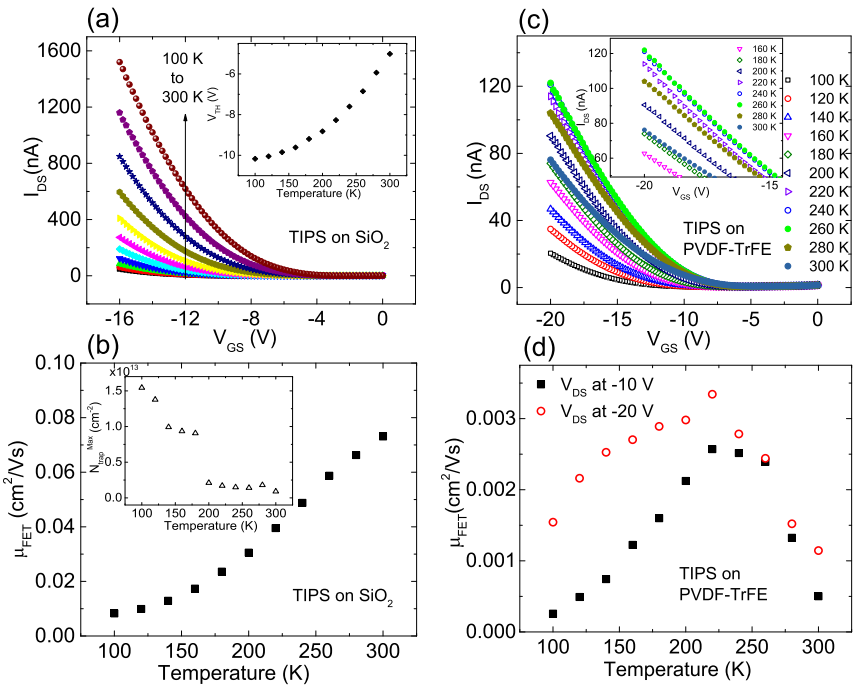

FIG. 3. Temperature dependent transconductance curves as a function of temperature from TIPS-pentacene FETs with (a) SiO_2 and (c) PVDF-TrFE dielectric layers. The inset in (a) shows the change in the threshold voltage as a function of temperature. (b) and (d) show the μ_{FET} mobilities as a function of temperature for SiO_2 and PVDF-TrFE dielectrics, respectively. The inset in (b) shows the trap density as a function of temperature, which were extracted from the subthreshold swing values. The carrier mobilities in (d) were extracted from two different transconductance curves, swept at V_{DS} = -10 V and -20 V.

traps, and k_B is the Boltzmann constant. Thermally activated transport in TIPS-pentacene has been observed by other groups with some nuances of temperature regimes [40] and dependence on the geometry of the device [5]. The above model is obviously more complex when the polarization field of the dielectric interface needs to be considered. As shown in Fig. 3(b), the SiO_2 based FET exhibits an enhanced mobility in the entire temperature range, whereas the PVDF-TrFE based FET shows decreased carrier mobility beyond $\sim$ 220 K. When the same PVDF-TrFE based device was swept at a higher voltage (till V_{DS} =V_G =-20 V), the extracted mobilities are higher (Fig. 3(d)) but the trend is the same as the -10 V data, namely, a decrease in the carrier mobility beyond 220 K is observed.

In order to understand the differences in transport mechanism in TIPS-pentacene FETs

with a non-ferroelectric dielectric versus a ferroelectric dielectric, we have measured the temperature dependence of the carrier mobility in TIPS-pentacene FETs with a variety of dielectrics and architectures. We have also used a bilayer dielectric SiO_2/PVDF-TrFE, shown in Fig. 1(b), where the interface property between TIPS-pentacene and the PVDF-TrFE layer is similar to the single layer PVDF-TrFE FET, except in the bilayer device the PVDF-TrFE layer does not act as a ferroelectric layer.

For a better visualization of FET carrier mobilities as a function of temperature, we plot the normalized values in Fig. 4(a). See Ref. [28] for the actual values of extracted mobilities as a function of temperature for the various dielectrics. In the temperature range of our measurements, the dielectric constant (k) of PVDF-TrFE roughly changes from 4 at 100 K to 8 at 300 K, as shown in the inset. Except for the PVDF-TrFE dielectric based FET, which reaches a maximum around 220 K, all other FETs show their highest mobility at 300 K. These features are reversible. Cycling the temperature few times results in a slight decrease of the carrier mobilities but the trends remain the same. A clear distinction is seen between bilayer (SiO_2/PVDF-TrFE) and single layer PVDF-TrFE FETs. It is important to realize that in the bilayer device since the SiO_2 layer is gated, PVDF-TrFE is not an active ferroelectric layer; the combined k is much smaller than for either of the dielectrics. Although in both FETs the interface between TIPS-pentacene and PVDF-TrFE is identical, the bilayer device does not show $d\mu/dT < 0$, suggesting that the ferroelectric nature of PVDF-TrFE is responsible for the negative coefficient of mobility beyond 220 K. Fig. 4(b) shows the Arrhenius plots of the FET mobilities in a temperature range of 100 K to 220 K, where the activation energies vary between 10 - 40 meV for the various dielectrics. We note that the activation energy reported for a printed PVP (TIPS-pentacene) FET was slightly higher compared to Fig. 4(b) as the temperature range over which the measurements were conducted was more restrained (160 K - 320 K) [41]. The data shown here for SiO_2 and CYTOP refer to the same TIPS-pentacene layer where the geometries were either top-gate or bottom-gate (Fig. 1(c)).

Prior work on ferroelectric FETs have shown that charge transport is strongly influenced by polarization fluctuation [21]. In the presence of a ferroelectric dielectric, the two competing effects as a function of temperature are a suppression of the charge carrier mobility in the ferroelectric phase (as a result of the coupling of the carrier to the dielectric polarization of the gate insulator) and an activated hopping transport responsible for enhancing μ_{FET}.

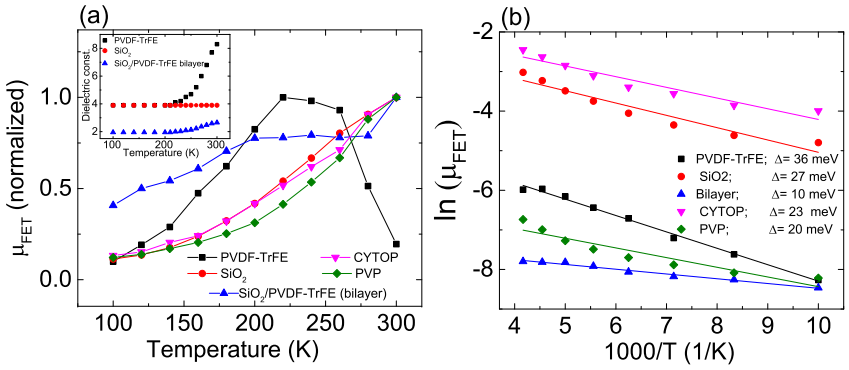

FIG. 4. (a) Normalized (to the maximum value) mobilities of TIPS-pentacene FETs as a function of temperature. The lines are a guide to the eye. The inset shows the variation of the dielectric constant of a few dielectrics as a function of temperature. (a) Arrhenius plots of TIPS-pentacene FET mobilities for various dielectric layers. The symbols are the experimental data and the lines are the fits. The bilayer refers to SiO_2/PVDF-TrFE.

Due to the constraints with temperatures above 320 K for TIPS-pentacene films, the full polarization effect of PVDF-TrFE cannot be explored in this work. The dielectric constant of PVDF-TrFE is greatly enhanced beyond 300 K, reaching close to 25 at $\sim$ 400 K [22]. The slightly higher activation energy of PVDF-TrFE compared with other dielectrics (seen in Fig. 4(b)) may be explained on the basis of a higher dynamic coupling between the charge carriers to the electronic polarization. Overall, the activation energies seen here in the low temperature range for the various dielectrics are similar to high mobility TIPS-pentacene FETs [6].

Several PVDF-TrFE single layer FETs were fabricated and they all showed a similar behavior in carrier mobilities seen in Fig. 3(d). Another batch of FETs was fabricated with PVDF-TrFE as the bottom-gate and CYTOP as the top-gate with the same TIPS-pentacene film being the active layer for both dielectrics. The PVDF-TrFE geometry entailed a bottom contact device. A distinct thermally activated transport is observed with CYTOP whereas with the PVDF-TrFE layer, a decrease in mobility is observed beyond 240 K [28]. The PVDF-TrFE layer in this dual geometry FET was 550 nm in comparison with the 430 nm thick layer in Fig. 3(c) and (d). The polarization field from a thicker ferroelectric layer is lower compared to a thinner layer (also observed in pentacene/PVDF-TrFE FETs [21]); hence, it is not surprising that the percentage decrease in mobility for the dual geometry

FET is lower compared to the device shown in Figs. 3 and 4. The connection between the polarization effect and the change in carrier mobility is elaborated in Section III B. In order to further elucidate whether the negative coefficient of mobility beyond 220 K in TIPS-pentacene is an inherent property of the semiconductor itself, we have conducted detailed temperature dependence from TIPS-pentacene diodes and compared them with pentacene diodes.

B. Diode characteristics: TIPS-pentacene versus pentacene

We used the two Au contacts across TIPS-pentacene (as shown in Fig. 1(e)) to measure the bulk current-voltage characteristics (hole current) as a function of temperature. This structure further ensures that we are using the same TIPS-pentacene film, with an identical trap distribution, as used for FET measurements. SCLC-based models have been used to study trap states in organic molecules and polymers for over 50 years. Shallow trapping with a single trap level was initially observed in pure polycrystalline organic molecules such as anthracene and naphthalene [42]. Subsequently, such discrete set of trap level SCLC has also been observed in semicrystalline blue-emitting ethyl-hexyl polyfluorene (PF2/6) conjugated polymers [43, 44], where regions of structural ordering is believed to be responsible for charge injection and transport.

Fig. 5(a) shows the current density (J) versus voltage (V) for hole carriers in a TIPS-pentacene diode. The $J-V$ curve (log-log plot) shows four distinct regions, characteristic of a one-carrier single set of traps. The first is the Ohmic region, where $J = (qn_0\mu V)/d$ with q being the charge, n_0 is the free carrier density, d is the thickness of film between the electrodes, and μ is the carrier mobility. The second region is SCLC trap-limited with the current density given by

$$J = \frac{9}{8}\epsilon\epsilon_0\mu\theta\frac{V^2}{d^3}. \tag{1}$$

In Eq.1, θ is the trapping fraction, ϵ is the dielectric constant of the polymer, and ϵ_0 is the permittivity of free space. For an exponential trap distribution, $J \propto V^m$ with $m > 2$. The third region in Fig. 5 where the current increases vertically is the trap-filled limit. The onset is the trap-filled voltage V_{TFL}, which is proportional to the density of traps (N_t)

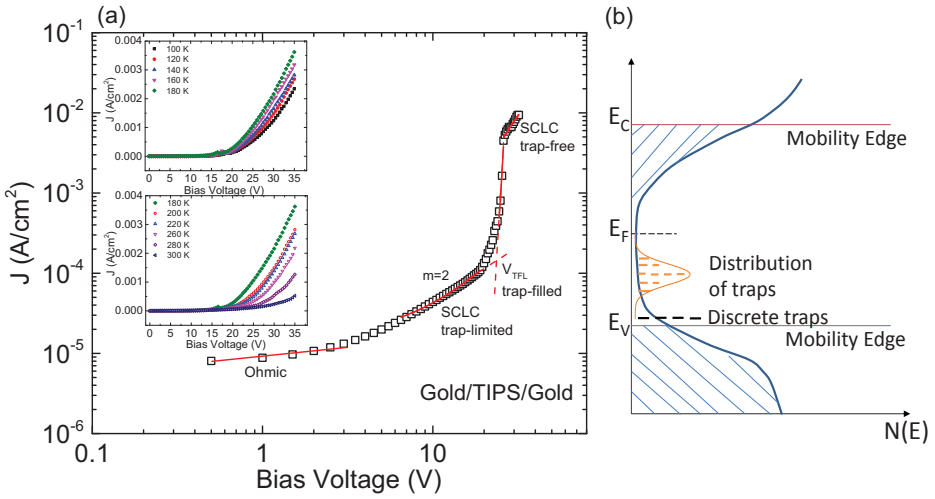

FIG. 5. (a) Current density versus voltage plot for TIPS-pentacene diode at room temperature. The J vs.V sweep shows all four distinct regions, characteristic of SCLC with discrete trap levels. The inset shows temperature dependent $J-V$ curves from 100 K to 180 K, and from 180 K to 300 K. (b) Schematic of the density of states in TIPS-pentacene.

$$N_t = \frac{3}{2}\frac{\epsilon\epsilon_0 V_{TFL}}{qd^2}. \tag{2}$$

The final region is the current only limited by the space charge and free from the influence of traps. The trap-free SCLC region is similar to the second region expressed by Eq. 1, with $\theta = 1$. Further, the trap energy (E_t) is related to the trapping parameter by $\theta = \frac{N_v}{N_t}\exp(-\frac{E_t}{k_BT})$, where N_v is the density of states within k_BT of the valence band edge.

The first run yields all the four regions as shown in Fig. 5(a); however subsequent voltage sweeps somewhat decreases the current. This is most likely due to the generation of additional traps while sweeping the voltage beyond V_{TFL}, which was also observed in PF2/6 [43]. To obtain the different parameters in Eqns. 1 and 2, one has to then resort to the very first run. From the trap-free SCLC region shown in Fig. 5(a), we obtain a carrier mobility of ~ 1.4 cm^2/Vs at room temperature. The second run yields more than an order of magnitude lower value of the mobility. The SCLC data were also confirmed from other Au/TIPS-pentacene/Au devices and from different runs of the same device [28]. We use the trap-free SCLC region to obtain μ at all temperatures. An average value of μ =0.08 $\pm$ 0.03 cm^2/Vs at 300 K was found by using the second or third sweep from different batches of

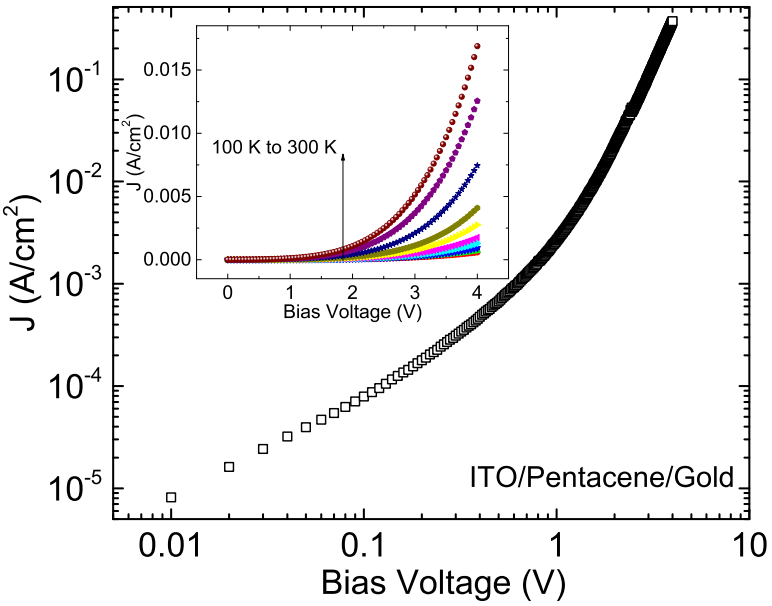

FIG. 6. Current density versus voltage plot for a pentacene diode at room temperature. The inset shows the temperature dependent $J-V$ curves from 100 K 300 K.

TIPS-pentacene diodes. More than the absolute values, we are interested in the trend in carrier mobilities as a function of temperature for obtaining insights into the bulk transport phenomenon.

Since PVDF-TrFE based pentacene FETs showed no negative coefficient of carrier mobility with temperature [21], we further compare the nature of the trap states in TIPS-pentacene with pentacene, and thus performed temperature dependent $J-V$ measurement from pentacene diodes as well. These diodes were grown by sandwiching a pentacene film between ITO and Au (in a vertical geometry), ensuring that it is predominantly hole transport. Fig. 6 shows the $J-V$ characteristics (log-log plot) from a pentacene diode at room temperature. Unlike TIPS-pentacene, discrete-trap SCLC is not observed. The SCLC follows a distribution of traps, which is typically seen in most π-conjugated molecules and polymers. With increasing temperature, the slope of the J-V curve continuously increases (as seen in the inset). Although trap-free SCLC is not observed, Eq. 1 fits the voltage range: 0.2 V to 1 V quite well from where we can then deduce the product of $\theta\mu$.

The hole mobilities extracted from the $J-V$ measurements by fitting the trap-free SCLC

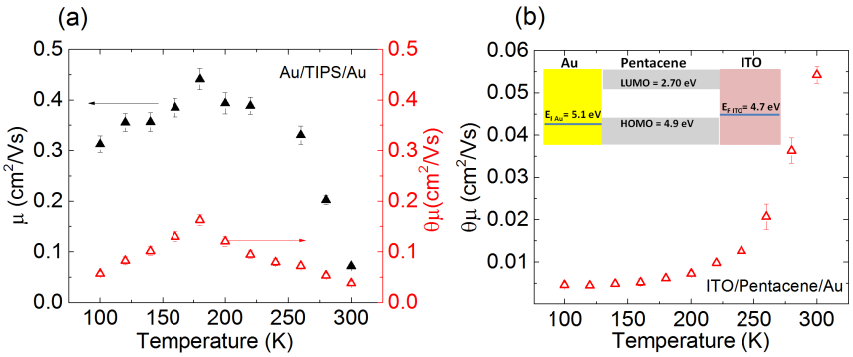

FIG. 7. (a) Hole mobility (filled triangles) as a function of temperature extracted from the trap free SCLC region in TIPS-pentacene diode. The open triangles show the product of the trapping fraction and carrier mobility in TIPS-pentacene extracted from the trap-limited SCLC region. (b) Product of the trapping fraction and carrier mobility as a function of temperature for a pentacene diode. The inset shows a schematic of the energy levels.

region with $J \propto V^2$ dependence in TIPS-pentacene are plotted in Fig. 7(a). Beyond 180 K, μ is seen to decrease with increase in temperature. These measurements have been repeated with several devices where the architecture was similar to Fig. 1(e), and the TIPS-pentacene was grown on different dielectrics (CYTOP, SiO_2, PVDF-TrFE). We point out that the dielectric layer plays no role in these measurements and that charge injection and transport is solely through the TIPS-pentacene film. Similar experiments from pentacene highlight that the $J-V$ curve does not show a single-trap SCLC behavior (Fig. 6). The trap-limited region agrees with $J \propto V^2$ dependence, from where we obtain the trends in mobilities with temperature. A cautionary remark here is that since the trapping fraction is unknown, we obtain the product of $\theta\mu$ from temperature dependent $J-V$ curves (plotted in Fig. 7(b). It is evident that μ increases with temperature even from the individual $J-V$ curves of the pentacene diode (see inset in Fig. 6). As an additional check, the product of $\theta\mu$ was also obtained for TIPS-pentacene from the trap-limited SCLC region, shown in Fig. 7(a). This product shows the same trend as μ.

Temperature-dependent $J-V$ measurements from two terminal devices allow an independent measure of transport in organic semiconductors without the influence of the dielectric. In comparing TIPS-pentacene to pentacene, we find that the $J-V$ diode characteristics are quite different; TIPS-pentacene distinctly shows a discrete trap behavior with all four

regions unlike pentacene. Furthermore, the hole mobilities in pentacene show a hopping transport with $d\mu/dT > 0$ in the temperature range of 100 - 300 K. High purity crystals such as anthracene and tetracene with discrete trap SCLC typically display a diminishing mobility with temperature (for both electrons and holes) [42, 45]. In tetracene, however, the decreasing mobility with temperatures beyond 180 K has been attributed to a phase transition [46]. Moreover, temperature dependence of the drift mobilities in crystals belonging to the acene family and other systems is strongly dependent upon the crystallographic directions [47]. The negative coefficient of mobility observed in TIPS-pentacene thus follows other molecular semiconductors that exhibit discrete trap SCLC behavior.

It is instructive to correlate the bulk mobility of pentacene with FET transport characteristics. Thermally activated transport in pentacene FETs (using non-ferroelectric dielectrics) has been observed by many groups [48–50]. Pentacene based FETs with PVDF-TrFE show two regimes in transport: polarization influenced as long as the dielectric is in the ferroelectric phase and then an activated transport when the dielectric is in the paraelectric phase [21]. In the ferroelectric phase, Fröhlich polarons play a role in suppressing the carrier mobility. The nature of transport in pentacene FETs agrees well with bulk transport (as seen from the diode characteristics here). Overall, the distribution of trap states in pentacene favors an activated transport. The weak-dependence of the charge carrier mobility (in pentacene FETs) in the ferroelectric phase of PVDF-TrFE is attributed to a polarization fluctuation driven transport.

The bulk transport properties in TIPS-pentacene is different from pentacene. A distinct discrete shallow trap SCLC is observed in TIPS-pentacene compared to the distribution of traps in pentacene. Beyond 180 K, a negative coefficient of mobility is observed. This is completely reversible upon cycling the temperature. Our results agree with the recent charge modulation spectroscopy results by Meneau *et al.* [6], where it is seen that charges become localized onto individual molecules in shallow trap states at low temperatures. Although the FET mobilities reported in this work are two to three orders of magnitude smaller than what is required to approach disorder-free limits, the temperature-dependence of carrier mobilities from PVDF-TrFE based FETs clearly shows $d\mu/dT < 0$ beyond 200 K, consistent with bulk transport measurements. The higher dielectric constant of PVDF-TrFE beyond 200 K (and under substantial electric fields) may partially reduce the trap depth due to screening, resulting in a de-trapping mechanism. This facilitates a transport through discrete traps,

as schematically shown in Fig. 5(b), which is manifested as band-like transport. Such a behavior is not observed in non-ferroelectric dielectric based FETs due to the lack of any polarization field and lower screening effects.

A high dielectric constant of the gate insulator thus results in a strong dynamic coupling of the charge carriers, mainly due to the Fröhlich polarons, which tends to suppress carrier mobilities as observed in pentacene FETs [21] and P3HT FETs [22]. The tunability of the dielectric constant of PVDF-TrFE with temperature allows a platform for changing the coupling between the charge carriers and the electronic polarization. Along with this coupling, the nature of the trap states also plays a role in dictating transport properties as seen in TIPS-pentacene FETs. Increasing the dielectric constant may enhance screening, reducing the trap depth, and thus facilitating transport through discrete trap states. This is manifested as a negative coefficient of carrier mobility with temperature in TIPS-pentacene FETs.

IV. CONCLUSIONS

Drop casted TIPS-pentacene films exhibit single-trap level SCLC, similar to high purity crystalline organic molecules. The origin of these traps could be structural or other chemical defects, which typically give rise to discrete trap states, and may occur at the grain boundaries. Bulk transport measurement from TIPS-pentacene clearly shows a negative coefficient of mobility beyond 180 K. A similar behavior is seen in FET transport when a ferroelectric dielectric, PVDF-TrFE, is used. As such the FET mobilities reported here are lower than the minimum condition mobility required for observing disorder-free transport, yet the presence of a polarization field of the ferroelectric dielectric results in a transport mechanism, exemplifying band-like transport above a certain temperature. We attribute this to an ease of a de-trapping mechanism owing to the nature of discrete traps. Ferroelectric dielectrics with the ability for tuning their polarization strength with temperature provide a mechanism for exploring different transport regimes in organic FETs. This work paves the way for exploring band-like transport ($d\mu/dT < 0$) in other solution processable π-conjugated molecules and polymers with discrete trap levels by utilizing ferroelectric dielectrics in FET geometries.

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