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Efficient and Hysteresis-Free Field Effect Modulation of Ambipolarly Doped Vanadium Dioxide Nanowires

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Abstract

The sub-picosecond metal-insulator phase transition in vanadium dioxide (VO_2) has attracted extensive attention with potential applications in ultrafast Mott transistors, which are based on electric field induced phase transition. However, the development of VO_2-based transistors lags behind, owing to inefficient and hysteretic gate modulation. Here we report ambipolar doping and strong field effects free of hysteresis in single crystalline VO_2 nanowires, synthesized via catalyst-free chemical vapor deposition. The ambipolarly doped VO_2 nanowires were achieved by controlling the oxygen vacancy density during the synthesis and showed strong gate effects because of their relatively low doping level. Both the doping type of the nanowires and the band bending direction at the metal-insulator domain walls were reversibly switched by electrochemical gating, as revealed by scanning photocurrent microscopy (SPCM). Furthermore, we eliminated the hysteresis in gate sweep via a hybrid gating method, which combines the merits of liquid ionic and solid gating. The capability of efficient field effect modulation of ambipolar conduction and band alignment offers new opportunities on understanding the phase transition mechanism and enables novel electronic applications based on VO_2.

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I. INTRODUCTION

Vanadium dioxide (VO_2), a strongly correlated electronic material, has been studied for decades due to its distinct metal-insulator transition (MIT) occurring slightly above room temperature (68°C) [1]. This abrupt phase transition that happens on the order of 100 fs [2] is accompanied by a resistance change of up to 5 orders of magnitude, which enables the potential application of thermochromic devices with switchable infrared reflectivity (smart windows) [3], ultrafast switches [4], and electronics superior to traditional silicon based transistors [5]. In particular, it has been proposed to integrate VO_2 into field effect transistors (FETs), often referred to as Mott transistors, which operate based upon an electrostatic control of the metal-insulator transition [5]. Although the carrier mobilities in strongly correlated materials are often much lower than that of silicon, their FET switching time is not determined by the carrier transit time but instead by the ultrafast metal-insulator transition time. The realization of the Mott transistors is challenging partially because the underlying mechanism of MIT in VO_2 is not yet clear. The MIT mechanism in VO_2 could be attributed to either the Mott model or the Peierls model. In the Mott mechanism, the carrier concentration plays an essential role in triggering the formation of a metallic phase, while in the Peierls mechanism the transition closely depends on the carrier-phonon interaction [6-8]. As of today, it still remains an open question which mechanism initiates the MIT in VO_2 [1].

To date, most previous research efforts were mainly focused on n-type VO_2 [9-12]. VO_2 is naturally n-type because of oxygen vacancies and can be doped by W^{6+} to further increase the electron concentration, which substantially reduces the phase transition temperature (T_c) [3, 13]. P-type VO_2 samples may provide additional insights on understanding the phase transition mechanism. For example, the hole-lattice coupling has been theoretically predicted to weaken/break V-V dimers in the monoclinic (M1) phase of VO_2, which may potentially lower T_c [14]. Moreover, as in most other semiconductor materials, the carrier type tunability of VO_2 is crucial for its applications in electronic and optoelectronic devices. Unfortunately, there have been very few reports of p-type VO_2 [15, 16] and all these reports are for polycrystalline thin films, where the phase inhomogeneity in the vicinity of T_c complicates optical and electrical measurements and leads to inconsistent results between samples. On the other hand, thanks to a large surface-to-volume ratio, nanostructures are superior to their bulk counterparts in terms of achieving ambipolar doping [17]. Single crystalline VO_2 nanowires (NWs), with their lateral dimensions smaller than the typical size of metallic and insulating domains (~1 μm), also offer an ideal platform to investigate the MIT process in VO_2. During the transition, simple one-dimensional (1D) domain structures can be stabilized along the axial direction of the NW, which simplifies the interpretation of the results and allows for a spatially resolved study of the electronic structures in the proximity of a domain boundary. However, the synthesis of p-type VO_2 NWs has not yet been reported in the literature to date.

In addition, the evidence supporting p-type VO_2 thin films in the previous reports was either Hall measurements [15] or indirect methods such as X-ray absorption spectroscopy

[16]. No field effect modulation of conductivity was shown in these previously reported p-type VO_2 samples. Direct field effect measurements not only provide critical information on carrier type, concentration, and mobility, but can also be used to control the carrier population and essential to achieving Mott transistors. Field effects in NWs are expected to be stronger than in thin films because of the reduced dimensions and small diameters. Field effect modulation of carrier concentration by conventional solid state gating has been demonstrated in n-type VO_2 NWs but turns out to be weak and hysteretic [12]. Due to the high carrier concentration and the consequent short Thomas-Fermi screening length in VO_2, conventional solid gating via the gate dielectric does not prove efficient enough in modulating the carrier concentration [12]. Electrochemical gating (or ionic liquid gating), although demonstrated capable of changing the conductivity by two orders of magnitude, usually suffers from large hysteresis [9-11, 18-21]. It was also discovered that the electrochemical gating likely induces a surface chemical reaction, including formation of oxygen vacancies [18] or hydrogenation [10, 22]. The electrochemical gating of VO_2 is in general composed of two regions. When the electrochemical gate voltage is low, the gating is purely electrostatic. Charge accumulates at both sides of the double layer forming an efficient capacitor. As the gate voltage further increases, chemical reactions occur and positive ions (K^+ or H^+) may intercalate into the VO_2 NWs which are balanced by the increased electron concentration in VO_2. In this region, the gate efficiency becomes even higher, leading to a phase transition in VO_2 associated with large change in conductivity. Unfortunately, this high

gate efficiency is often associated with slow and irreversible chemical reaction at the VO_2 surface, causing large hysteresis which prevents the realization of fast transistors.

Here, we report the synthesis of p-type VO_2 NWs by controlling the oxygen vacancy concentration during the NW growth. The carrier type is directly determined by field effect and scanning photocurrent microscope (SPCM) measurements. We then demonstrate that the carrier type can be reversibly switched via thermal annealing or electrochemical gating, as evidenced by the gate dependent conductivity and the flipping of the photocurrent polarity at the metal-insulator domain walls as well as the NW-electrode Schottky junctions. Finally, we introduce a hybrid gating technique that can achieve efficiency similar to the traditional electrochemical gating, while substantially suppressing the hysteresis of the gate sweep and increasing the switching speed of VO_2 devices.

II. SYNTHESIS OF AMBIPOLAR VO_2 NANOWIRES

VO_2 NWs were synthesized via a chemical vapor deposition (CVD) method using V_2O_5 as the precursor in a tube furnace (Lindberg Blue M). V_2O_5 (Alfa Aesar, 99.99%) powder was adopted as the only precursor and placed in a quartz boat at the center of the tube furnace. Polished/unpolished x-cut quartz substrates (MTI) were placed 7 cm downstream from the boat, as shown in Fig. 1(a). The system was first pumped down to a base pressure of ~100 mTorr, then injected with Ar at a flow rate of k_{Ar} = 0 ~ 60 sccm to vary doping concentration. The pressure under Ar flow ranged from 0.1 ~ 0.9 Torr. The furnace was heated up to 880°C and maintained at the peak temperature for 30 minutes to 2 hours.

During the growth, the decomposition of V_2O_5 generates O_2. By varying the Ar flow rate, the partial vapor pressure of O_2 can be controlled, which affects the carrier type and concentration in the NWs. Because the substrate temperature was kept above the melting point of V_2O_5 (690°C), solid V_2O_5 structures were prohibited from growing on the substrate. Immediately after the growth, the furnace was quickly cooled down to room temperature for a rapid termination of the reaction to avoid generation of the V_2O_5 phase.

The VO_2 NWs grown on the unpolished surface of the quartz substrate were dense and free-standing [Fig. 1(b)], while the growth on the polished quartz surface consisted of NWs and nanoplates, which were partially embedded in the substrate [Fig. 1(c)]. It has been demonstrated that the rough quartz surface favors the nucleation of VO_2 particles [Fig. S1] and leads to free standing VO_2 NWs [23]. NWs grown on the polished quartz substrates tended to align with the crystal orientation of the x-cut quartz [24], as shown in the inset of Fig. 1(c). Moreover, an interesting pattern of alternating metal-insulator domains on these VO_2 nanoplates was observed at ~70 °C, as shown in Fig. 1(c). The angle between the stripes of the domains and the long axis of the nanoplates was measured to be 42 ± 2° for all the nanoplates. Previously, an angle of 57° has been reported in epitaxially grown VO_2 thin films on TiO_2 substrates, and attributed to the monoclinic-rutile crystal symmetry breaking [25]. The different angle observed here was likely related to the strain distribution in NWs grown on the different types of substrates, which affects the local phase transition temperature [26, 27]. Further studies are necessary to understand this interesting behavior.

The growth on the unpolished quartz substrates consists of both large microbeams ($d > 1$ μm) and thin NWs ($d < 300$ nm). Compared to previously reported CVD-grown microbeams [28], the thin NWs with increased surface-to-volume ratio are beneficial for obtaining a stronger gate response. The NWs grown on unpolished surfaces are free-standing and easy to transfer to device substrates. These devices also exhibited longer domains during the MIT, ideal for investigating the domain walls by SPCM. Therefore, we focus on the NWs on the unpolished surfaces for further experiments throughout this work. To further characterize the structure and phase of these NWs, we perform selected area electron diffraction (SAED) on a transmission electron microscope (TEM). To transfer these NWs onto a TEM grid, the growth substrate was placed in a beaker containing ethanol solution and was sonicated subsequently. Then, 0.5 micro-liter of the solution was transferred with a pipette on a TEM grid covered with carbon thin films to support the wires. Fig. 1(d) shows a TEM image of a typical VO_2 NW. The uniform SAED pattern throughout the entire NW confirms the single crystalline nature of our NWs. The NW growth direction was along the [100] direction of the VO_2 monoclinic (M1) phase. X-ray diffraction (XRD) peaks (Fig. 1(e)) of the NWs matched the M1 phase of VO_2 (PDF#44-0252) and no other phases, such as V_2O_5, were observed.

In order to fabricate single NW field effect transistors (FETs), the free-standing NWs were transferred onto 300 nm SiO_2 coated, heavily p-doped Si wafers by directly pressing the Si wafer against the growth substrate. Subsequently, top metal contacts (250 nm Cr / 50 nm Au) were made to individual NWs using electron beam lithography and electron beam evaporation. The top contacts functioned as source and drain electrodes, and the Si

substrate served as the back gate. An SEM image of a single NW FET is shown in Fig. 1(f). These FETs all exhibited linear current vs. source-drain voltage (I-V_{SD}) curves. Four probe measurements demonstrated that the contact resistance was less than 1% of the NW resistance and could be ignored. The temperature dependence of the conductance of a typical device is shown in Fig. 1(g), which exhibits a 4 order of magnitude change across $T_c \approx 68$ °C, indicating an abrupt MIT in this sample. Varying from sample to sample, the transition temperature from the insulating phase to the metal phase (estimated as the temperature at which the entire conduction channel becomes metallic) ranged from 66 °C to 150 °C. The transition curve of another device with higher T_c and a histogram of T_c distribution can be found in Fig. S2. We did not find a clear correlation between T_c and doping type/concentration. The difference in T_c is most likely caused by the strain effects from the substrates and electrodes.

The conductivity of these NWs at room temperature (0.6 S m^{-1}) was much lower than previously reported n-type devices [23, 28, 29], indicating a lower carrier concentration in these NWs. To further characterize the carrier type and concentration in these NWs, we applied a back gate voltage to our devices and measured the field effect response of these NWs. The conductance modulation of a typical NW with a diameter of 240 nm grown at k_{Ar} = 0 sccm was shown in Fig. 2(a). The reasonably small hysteresis [12] and the downward slope clearly reflected the p-type nature of this device. The carrier concentration and mobility were extracted as $p = 2\times10^{18}$ cm^{-3} and $\mu = 0.04$ $cm^2/(V\cdot s)$, by using a gate oxide capacitance estimated from the device geometry. We measured more than 40 single-NW FET devices

grown at different Ar flow rates. The results showed that at k_{Ar} = 0 sccm, all NWs were p-type; at k_{Ar} = 30 sccm, we had a mixture of p-type and n-type NWs; and at k_{Ar} = 60 sccm, all NWs were n-type (an n-type gate scan was shown in Fig. S3). Solid gate response in VO_2 nanostructures is known to be weak with a slow response, even when using a high-κ dielectric [12]. In comparison, the p-type VO_2 NWs showed a much stronger gate modulation with a 50% conductance change and a much faster gate response. This is likely caused by the smaller diameters and lower carrier concentrations in the p-type VO_2 NWs.

III. GATE TUNABLE BAND BENDING AT DOMAIN BOUNDARY

We then performed SPCM measurements on the p-type NW devices in ambient environment. SPCM provides spatially resolved photocurrent mapping and has been used to explore charge carrier transport and recombination in various nanostructures [17, 28, 30-32]. The detailed experimental setup can be found in our previous work [28, 33]. Briefly, a 532 nm CW laser was focused by a 100× N.A. 0.95 objective lens to a diffraction limited spot and raster scanned on a planar NW device by a pair of mirrors mounted on galvanometers, while both the reflection and the photocurrent signals were simultaneously recorded to produce a two-dimensional (2D) map of the photocurrent. The laser intensity was controlled below the threshold of the insulator-to-metal transition for all measurements below. Under room temperature and V_{sd} = 0 V, the photocurrent image near a NW contact showed a single localized spot [Fig. 2(b)], which we attributed to the photovoltaic effect caused by the Schottky junction at the contact. The polarity of this contact spot indicated a downward band bending from the VO_2 NW towards the Cr electrode, as shown in the schematic drawing in

Fig. 2(b), which is consistent with the p-type nature of the NWs. In comparison, our previous SPCM measurements showed an opposite band bending direction in devices incorporating n-type VO_2 NWs grown by using VO_2 powder instead of V_2O_5 [28].

As the temperature was ramped to T = 95 °C, multiple metal/insulator domains emerged along the NW, as shown by the optical reflection image in Fig. 2(c). The photocurrent image at V_{sd} = 0 V showed a localized spot on each domain boundary with alternating polarities. The polarities were all consistent with the band bending of a Schottky junction between a metal and a p-type semiconductor, as shown in the schematic drawing of Fig. 2(c). The band bending direction at the domain wall is also opposite to the measurements performed on n-type VO_2 NWs [28]. At V_{sd} = 20 mV, the photocurrent patterns extended to the entire insulating domains, as the external electric field dissociates the photo-injected electrons and holes at any position along the insulating domain of the VO_2 NW [34]. The photocurrent was negligible on the metallic domains since the voltage drop was mostly on the insulating domains.

We have attributed the origin of the observed photocurrent to the photovoltaic effects, where the electric field at the domain walls or contact junctions separates photo-injected electrons and holes and leads to photocurrent. Note that in a previous report, the photocurrent spots at the domain boundaries of VO_2 nanobeams were attributed to thermoelectric effects, where the laser heating induces a temperature gradient along the NW driving an electric current [29]. In the previous report, the photocurrent spots were extended along the nanobeam by a few microns. This is expected in thermoelectric effects as the temperature

decays away from the laser spot with a characteristic thermal decay length of a few microns. The photocurrent spots observed in this letter, however, were much more localized than the thermal decay length, indicating a different origin. We further confirmed that the thermal decay length in our VO_2 NWs was indeed long by measuring the metal domain length induced by local laser heating at different intensities, as detailed in the Supplementary Material (Fig. S4) [35]. Moreover, the magnitude of the photocurrent spots at junctions were enhanced (suppressed) by a reverse (forward) bias (Fig. S5), consistent with the expected Schottky electric field change under bias [34]. We thus concluded that the origin of the photocurrent in our VO_2 NWs was most likely photovoltaic rather than thermoelectric. This different dominating photocurrent mechanism is likely caused by the differences in doping levels of the p-type NWs, which ultimately modulates the Seebeck coefficients and band alignment. A recent report showed that both photovoltaic and thermoelectric effects can play a role in generating photocurrents in VO_2 NWs [36].

Fig. 3 shows the evolution of photocurrent patterns as a function of temperature. As the temperature was ramped from T = 74 °C to T = 137 °C, the metallic domains (M) grew and insulating domains (I) shrunk (domain 1) or disappeared (domain 2). The persistent insulating domains at temperature significantly above the bulk T_c are likely due to the tensile stress induced by the partial insulator to metal transition in the NW. The phase transition from insulator to metal causes a ~1% shrinking along the NW axis, which leads to tensile stress in the remaining insulating segment of the NW and increases its T_c. Surprisingly, during this process the photocurrent spots on the domain boundaries first became weaker, and eventually

switched polarity, as shown in Fig. 3(b, c). After we lowered the temperature, the photocurrent spots flipped back to the original direction. The reversal of the photocurrent direction at high temperature was consistently observed in all measured devices, with the switching temperature varying slightly from 110 °C to 137 °C. If the same band bending was preserved, a higher photocurrent should be expected at higher temperature, because the device resistance was significantly reduced. The smaller photocurrent at T = 74 °C indicates a reduction of the band bending, hence a weaker electric field at the Schottky junction of the domain wall. The eventual reversal of the photocurrent direction at T = 137 °C suggests a band bending flipping, which indicates a significant change in carrier concentration and likely a change in carrier type. Such a change may be caused by the formation of oxygen vacancies at high temperature. It has been reported that rapid thermal annealing at 723 K in vacuum for tens of seconds leads to an oxygen deficiency and heavier n-doped VO_{2-x} with a substantially reduced T_c [37]. Though our annealing temperature is much lower than that in the report, the oxygen desorption can still create oxygen vacancies, most likely at the surface, and the consequent doping change can induce a band bending flipping. As we lower the temperature, oxygen can be re-adsorbed to the NW and the polarity switching is thus reversible.

Next we demonstrate the field effect modulation of the band bending and carrier type in the p-type VO_2 NWs by an electrochemical gating method. To fabricate the electrochemical gate, an ionic liquid droplet of polyethylene glycol (PEO, Alfa Aesar) with 5 wt% of $KClO_4$ was applied to the NW device by a micromanipulator, as shown in Fig. 4(a). By controlling

the amount of PEO applied to the tip of the micromanipulator, we achieved a small liquid drop with a size of 20 – 100 μm. The temperature was kept at T = 35°C which was slightly above the melting point of the droplet. As shown in Fig. 4(b), when the liquid ionic gate voltage V_g^L was increased, the conductance first decreased and then increased. The initial reduction in conductance was consistent with the p-type behavior as obtained with the solid state gating. When V_g^L was further increased, the liquid gate switched from the electrostatic operational region to the electrochemical operational region. More electrons were injected to the NW, which resulted in a steep upward slope in the gate scan, indicating n-type doping. In order to further confirm the carrier type switching from p-type to n-type, we examined the photocurrent spots at the metal-insulator domain boundaries and the NW-electrode contacts upon changing V_g^L. At both locations, the photocurrent spots switched polarities, as shown in Fig. 4(c, d). The photocurrent against V_g^L was plotted in Fig. 4(e), which followed a similar trend as the conductance change in Fig. 4(b). The photocurrent polarity switching was reversible and its sign switched back after the removal of V_g^L. As the Fermi level of the metal domain is expected to be insensitive to gating, the band bending flipping is caused by the Fermi level shift-up induced by the positive electrochemical potential in the insulator domain. Electrochemical gating likely only injects K^+ or H^+ ions near the surface of the VO_2 NWs, which leads to a radial doping gradient with an n-type shell and a p-type core. Such a core/shell structure is consistent with a non-zero minimum conductance as the gate voltage switches the NW from p-type to n-type [Fig. 4(b)]. If the NW has a uniform carrier concentration, a near zero conductance is expected as the gate voltage shifts the Fermi level

across the mid-gap. The shell and core have opposite band bending direction near the metal and the shell eventually dominates as the gate voltage is increased, resulting in a reverse of the photocurrent direction. This observation clearly demonstrates that electrochemical gating can efficiently shift the Fermi level in the insulator domain of the VO_2 NWs and switch the carrier type.

IV. HYBRID GATING

Despite its high efficiency compared to solid gating, the ionic liquid gating suffers from considerable hysteresis [Fig. 4(b)], which is caused by the slow and irreversible electrochemical reaction happening across the electron double layer (EDL) at the NW surface. In fact, if we try to further increase the conductance by applying a higher V_g^L, the reaction quickly becomes irreversible and results in much more pronounced hysteresis, as shown in Fig. 5(c). Such hysteresis is a common problem in a VO_2 ionic liquid FET as it limits its prospective application towards ultrafast transistors [9-11, 18]. In order to suppress the hysteresis, we introduce a new hybrid gating technique as depicted in Fig. 5(a). In this new setup, the gate voltage was applied to the back silicon yet with an ionic liquid droplet covering the NW device. The effective circuit diagram is drawn in Fig. 5(b). The potential reference point is chosen to be the drain side of the NW. The source-drain voltage applied is much smaller than the gate voltage, thus the source/drain electrodes can both be regarded as the grounding point. Besides the usual solid gate capacitor (C_S), the ionic liquid droplet formed an additional set capacitors in parallel to C_S. The droplet formed one capacitor ($C_{EDL(NW)}$+$C_{EDL(ET)}$) with the NW/electrode surface while forming another capacitor (C_{LS})

with the submerged SiO_2 surface. The two sets of capacitors C_{LS} and $C_{EDL(NW)}$+$C_{EDL(ET)}$ were in series, as shown in Fig. 5(b). With realistic parameters (Table S1) in our experimental setup, the magnitudes of these capacitors were estimated to be $C_S \approx 10^{-15}$ F, $C_{EDL(NW)} \approx 2.5\times10^{-14}$ F, $C_{EDL(ET)} \approx 2\times10^{-13}$ F, $C_{LS} \approx 8\times10^{-14}$ F. Therefore we have $C_S << C_{LS} << C_{EDL(NW)} + C_{EDL(ET)}$. With a gate voltage V_g^H applied to the back gate, the total charge injected to the NW is

$$Q = C_S V_g^H + \frac{C_{LS}\left(C_{EDL(NW)}+C_{EDL(ET)}\right)}{C_{LS}+C_{EDL(NW)}+C_{EDL(ET)}} \cdot V_g^H \cdot \frac{C_{EDL(NW)}}{C_{EDL(NW)}+C_{EDL(ET)}} \approx \frac{C_{LS}C_{EDL(NW)}}{C_{EDL(ET)}} V_g^H \quad (1)$$

Compared to the solid gating case where $Q = C_S V_g^H$, the charge injection efficiency has increased by a factor of $C_{LS}C_{EDL(NW)}/C_{EDL(ET)}C_S \approx 10$. In addition, when V_g^H is scanned back to zero, the potential difference across the capacitor C_{LS} offers a counter voltage which assists the discharge of the EDL through an inverse electrochemical reaction. The series capacitor C_{LS} hence protects the NW from irreversible chemical reaction and greatly reduces the hysteresis in the gate scan.

The reaction equations are

$$x(K^+ + e^-) + VO_2 \xrightarrow{\text{charge}} K_xVO_2, \quad K_xVO_2 \xrightarrow{\text{discharge}} x(K^+ + e^-) + VO_2 \quad (2)$$

These two reactions are accompanied by the charging/discharging through the EDL. The charging occurs when the gate voltage is above a certain threshold V_{th} and the discharging occurs when the gate voltage is decreased below a threshold. When these reactions happen, the EDL should no longer be modeled as a pure capacitor, but with a leakage resistor in parallel, as illustrated in Fig. 5(c)-(e). For simplicity, we have omitted the irrelevant C_S and

combined $C_{EDL(NW)}$+$C_{EDL(ET)}$ as C_{EDL}. C_{EDL} corresponds to electrostatic charging while r_{EDL} is associated with the electrochemical reaction. The value of r_{EDL} can be evaluated by the gate leakage current during the liquid gate scan. The leakage current is below the detection limit of the instrument when V_g^L < 2V and reaches a maximum of 0.5 nA when V_g^L = 3 V, corresponding to r_{EDL} = 6 GΩ. With the auxiliary capacitor C_{LS} in series, when decreasing the gate voltage V_g^H, the charge stored on the C_{LS} and its associated potential difference will then push a reversed current through r_{EDL} as shown in Fig. 5(e) and lead to a reversal of the chemical reaction. Thus, C_{LS} drives fast extraction of K^+ from the VO_2. Note that the voltage on the EDL also flips sign during this discharge process. On the contrary, if there is no C_{LS}, lacking of the driving force from C_{LS}, the extraction of K^+ from the VO_2 may take a much longer time, causing the large hysteresis. The function of the capacitor C_{LS} is analogous to a spring attached to a mechanical system, making the extraction of K^+ much faster and suppressing the hysteresis. It provides a restoring force (counter voltage) such that when the external driving force is removed, the system can return to its original position.

The experimental results with the traditional liquid gating and our new hybrid gating technique are compared in Fig. 5(f) and (g) respectively. While both setups were able to induce a 2 order-of-magnitude change in the conductance, the hybrid gating technique allowed for a much faster scan speed and resulted in a much smaller hysteresis than the traditional liquid gating. The photocurrent polarity switching presented earlier can also be induced by this hybrid gating technique, as shown in Fig. S6. This hybrid gating method with

strong field effects free of hysteresis is highly desirable in realizing VO_2 based transistors with high speed and may find applications in systems beyond VO_2 as well.

V. CONCLUSIONS

In conclusion, we have synthesized single crystalline p-type VO_2 NWs through the control of oxygen partial pressure during the growth. The p-type nature of these NWs is confirmed by both solid state gating and electrochemical gating methods, and the photocurrent polarity at Schottky junctions. The low doping level in p-type NWs enables strong gate effects. Annealing at temperature above 110 °C leads a switching of the photocurrent polarity, indicating a band bending direction change. Photocurrent polarity at the contact Schottky junctions and the metal-insulator domain boundaries flips sign when an electrochemical gate voltage is applied, manifesting an efficient control of the Fermi level in the insulating domain of the VO_2 NWs. A new hybrid gating technique is demonstrated to greatly suppress the hysteresis of the field effect response while maintaining a similar efficiency as the traditional ionic liquid gating. The efficient and hysteresis free field effect modulation of ambipolar conduction in VO_2 NWs offers new opportunities to investigate the fundamental phase transition mechanism and paves the way to the development of novel electronic devices based on this strongly correlated material.

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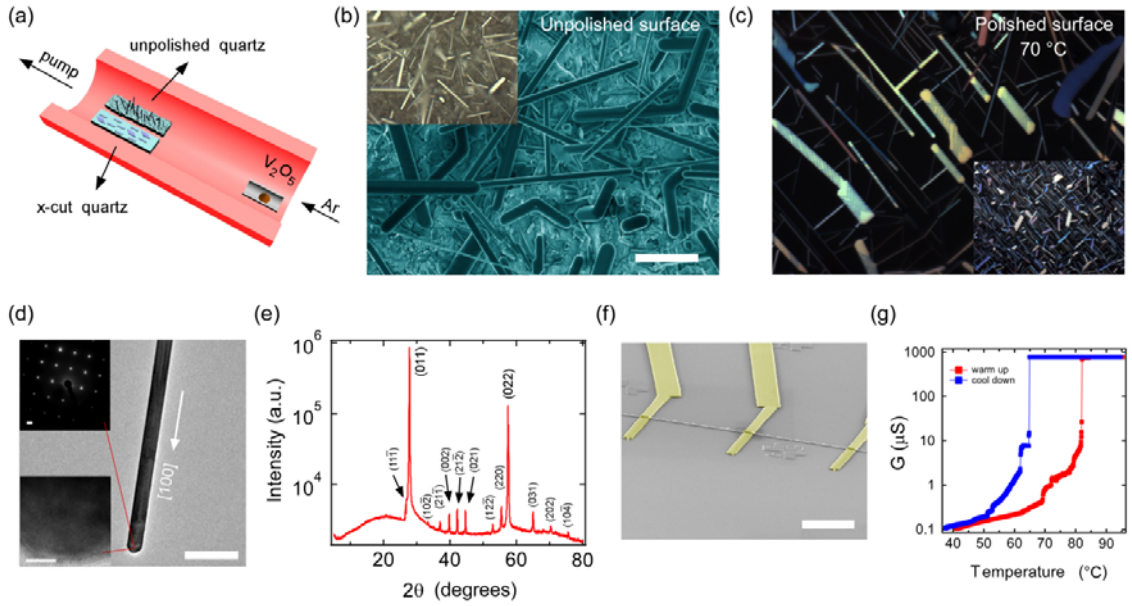


FIG. 1. Synthesis and characterization of p-type VO_2 NWs. (a) Schematic drawing of the CVD setup. (b) SEM image of the VO_2 NWs on an unpolished quartz substrate. Scale bar: 4 μm. Inset: optical microscope image of the same substrate showing free-standing NWs. (c) Dark field optical microscope image of VO_2 NWs and nanoplates with stripes of metallic domains on a polished quartz substrate at 70 °C. Inset: low-resolution image of the same substrate showing self-alignment of the NWs. (d) TEM image of a single VO_2 NW. Scale bar: 0.5 μm. Upper inset: selected area electron diffraction (SAED) patterns showing monoclinic structure over the entire region. Scale bar: 1 nm^{-1}. Bottom inset: high-resolution TEM image of the NW. Scale bar: 10 nm. (e) XRD pattern of VO_2 NWs obtained from the as-grown unpolished quartz substrate. (f) SEM image of a single VO_2 NW FET. Scale bar: 10 μm. (g) Conductance of a single VO_2 NW as a function of temperature. The applied bias is 10 mV to avoid Joule heating effect.

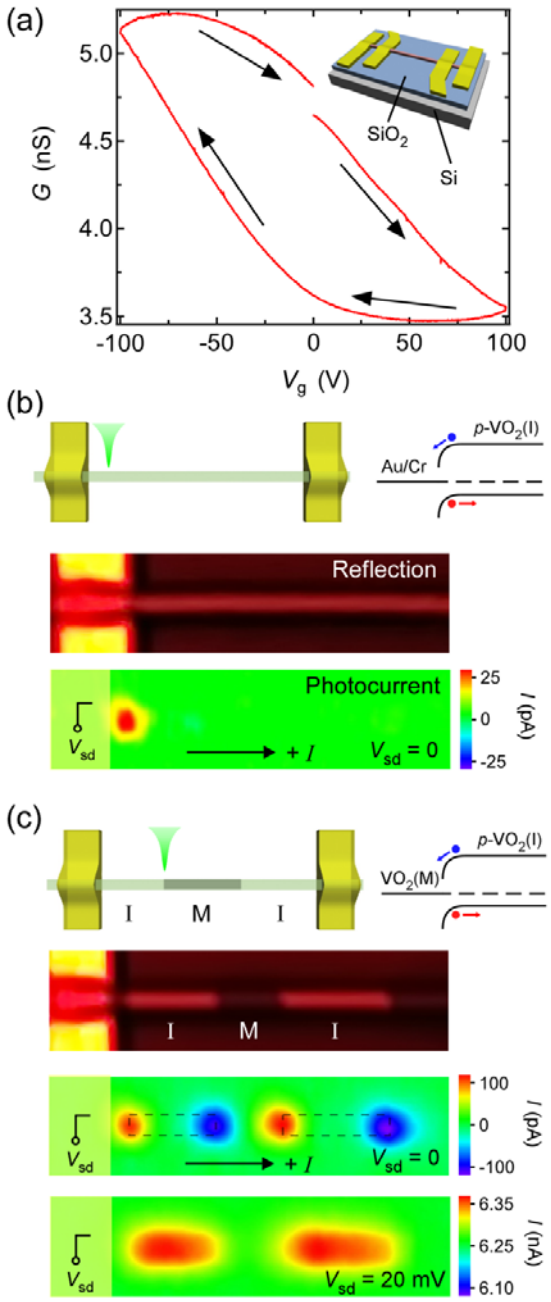


FIG. 2. SPCM characterization of a single p-type VO_2 NW FET. (a) Solid gate sweep of a single NW device showing p-type conduction. The arrows indicate scan direction. The fixed source-drain bias voltage is 0.5 V. The gate scan speed is 0.75 V/s. The linear part in the middle of the curve is employed for the extraction of mobility. Inset: schematic drawing of the device configuration. (b) SPCM measurements of the VO_2/Cr Schottky junction at 25 °C. (c) SPCM measurements of a VO_2 NW device with coexisting metal (M) and insulator (I)

domains at 95 °C. The upper and bottom photocurrent images are obtained at V_{sd} = 0 and 20 mV, respectively. For (b) and (c), at the top shows schematic drawings of the experimental setup and band diagrams of the junction; in the middle is the reflection image; at the bottom are the photocurrent images. The scale bars denote 2 μm. The laser peak intensity is 2.5 kW/cm^2.

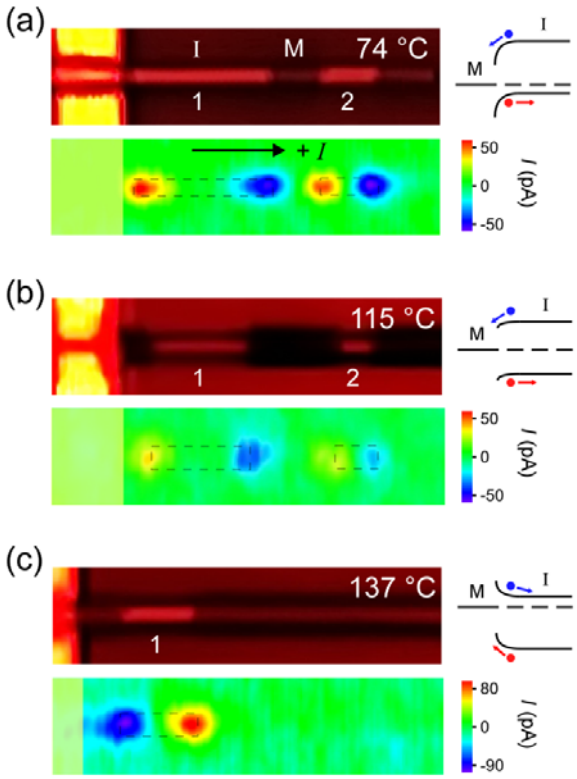


FIG. 3. Temperature induced photocurrent polarity switching at metal-insulator junction. All the photocurrent images in this figure are acquired at V_{sd} = 0 mV and laser intensity of 2.5 kW/cm^2. (a) SPCM measurements at 74 °C showing two insulator domains. (b) SPCM measurements at 115 °C showing two insulator domains and weaker photocurrent spots. (c) SPCM measurements at 137 °C showing only one insulator domain and flipped photocurrent spots at the metal-insulator junctions. For each panel, at the top shows the reflection images and band diagrams of a M-I junction; at the bottom shows the photocurrent images.

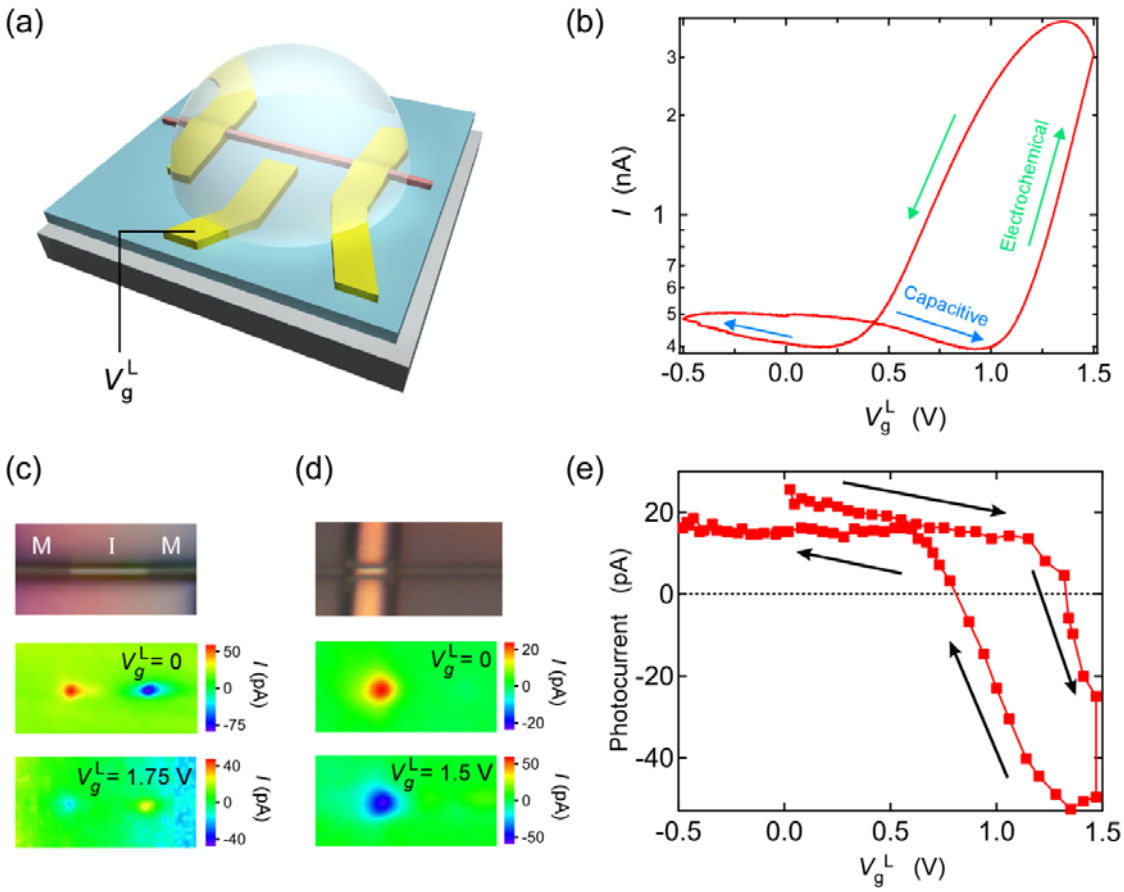


FIG. 4. Electrochemical gating induced photocurrent polarity switching at metal-insulator and Schottky junctions. (a) Schematic drawing of the three-terminal electrochemical gating setup. (b) A typical electrochemical gate sweep of single VO_2 NW device. The gate voltage scan speed is 10 mV/s. (c) SPCM measurements of a VO_2 NW with coexisting metal and insulating domains at V_g = 0 and 1.75 V, respectively. The measurements are conducted at 70 °C. (d) SPCM measurements a VO_2 NW with Cr/Au contacts at V_g = 0 and 1.5 V, respectively. The measurements are performed at 30 °C. (e) Photocurrent as a function of the liquid gate voltage. The photocurrent is measured by fixing the laser spot near the contact. The gate scan speed is the same as (b). V_{sd} = 0.1 V in (b) V_{sd} = 0 V in (c)-(e).

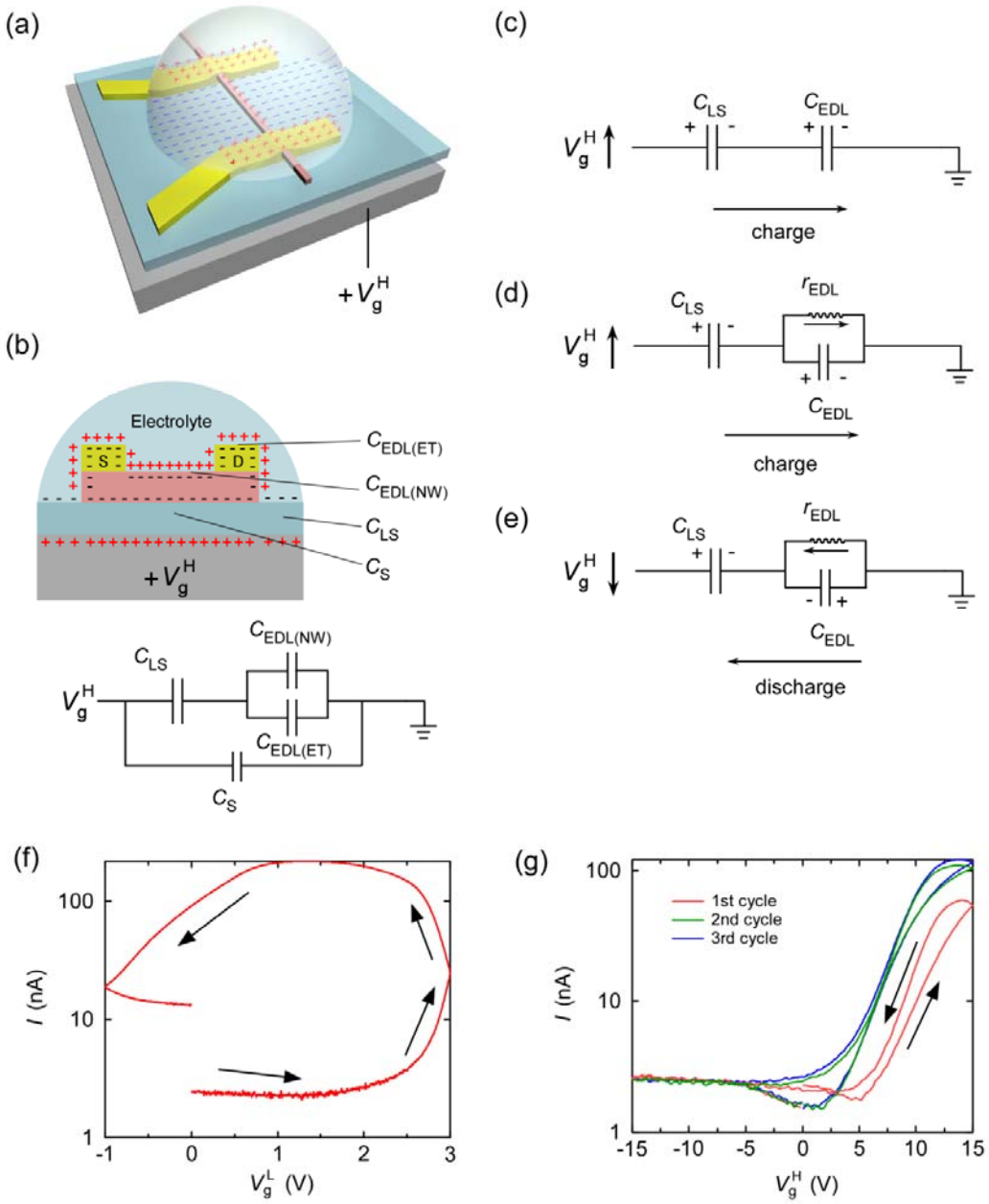
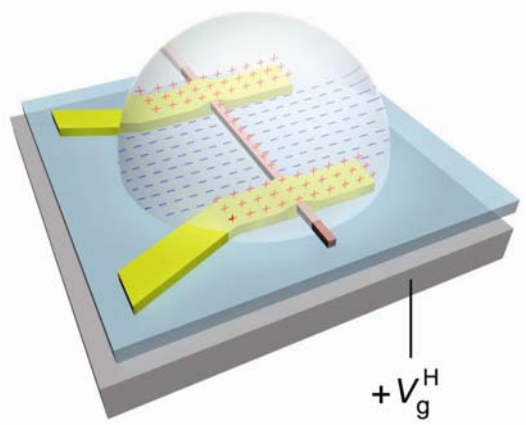


FIG. 5. Hybrid gating of a single VO_2 NW device. (a) Schematic drawing of the hybrid gate setup and charge distribution when a positive V_g^H is applied to the back gate. (b) Schematic drawing of the cross section of the hybrid gate setup. Bottom: equivalent circuit model of the setup. (c)-(e) Effective circuit diagrams illustrating the mechanism of hysteresis suppression. For simplicity, we have omitted the irrelevant C_S and combined $C_{EDL(NW)}$+$C_{EDL(ET)}$ as C_{EDL}. (c) When V_g^H increases but $V_g^H < V_{th}$, the EDL serves as a pure capacitor. (d) When V_g^H

increases and $V_g^H > V_{th}$, the EDL switches into the electrochemical operational region and there is a persistent leakage current through the EDL. (e) When V_g^H decreases, the charge stored in capacitor C_{LS} applies a counter voltage which pushes a reversed discharging current through the EDL. (f) Liquid gate sweep between -1 V and +3 V. The arrows indicate scan direction. The scan speed is 50 mV/s. (g) Hybrid gate sweep between -15 V and +15 V at 500 mV/s. V_{sd} = 50 mV for both (f) and (g).

Key Image:



Teaser:

The development of VO_2-based transistors lags behind, owing to inefficient and hysteretic gate modulation. Here, we report ambipolar doping and strong field effects free of hysteresis in single crystalline VO_2 nanowires via a hybrid gating method.