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Representation and design of wavelets using unitary circuits

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The representation of discrete, compact wavelet transformations (WTs) as circuits of local unitary gates is discussed. We employ a similar formalism as used in the multi-scale representation of quantum many-body wavefunctions using unitary circuits, further cementing the relation established in Refs. 1 and 2 between classical and quantum multi-scale methods. An algorithm for constructing the circuit representation of known orthogonal, dyadic, discrete WT is presented, and the explicit representation for Daubechies wavelets, coiflets, and symlets is provided. Furthermore, we demonstrate the usefulness of the circuit formalism in designing novel WT, including various classes of symmetric wavelets and multi-wavelets, boundary wavelets and biorthogonal wavelets.

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I. INTRODUCTION

The development of compact, orthogonal wavelets[3–6] represents one of the most significant advances in signal processing from recent times[7–9]. Like well established methods based on Fourier analysis, wavelets can be employed to obtain a compressed representation of spatially or temporally correlated data, and thus have found significant applications in image, audio and video compression [10–12]. By providing a multi-resolution analysis, a WT can capture correlations over many different length/time scales, which is key to their usefulness in practical applications.

Similarly, multi-scale methods, in the context of the renormalization group (RG) [13], which provides a systematic framework to implement changes of scale in many body systems, have also had a long and successful history in the context of condensed matter physics and quantum field theories. A recent advance in RG methods for quantum many-body systems is the multi-scale entanglement renormalization ansatz (MERA)[14, 15], where quantum many-body wavefunctions are represented as circuits comprised of local unitary gates. By properly encoding correlations at all length scales, MERA have been demonstrated to be particularly useful in the numerical investigation of quantum many-body systems where many scales of length are important, such as in systems at the critical point of a phase transition[16–23].

While the conceptual links between WT and the RG have been previously examined[24], more recently it was shown that a WT acting in the space of fermionic mode operators corresponds precisely to a MERA[1, 2]. This wavelet/MERA connection proved useful in allowing construction of the first known analytic MERA for a critical system, and may further prove useful in understanding e.g. the scaling of errors in MERA. The purpose of this paper is to take the connection the other way, and examine whether the tools and ideas developed in the con-

text of the MERA are useful in the understanding and design of WTs. Specifically, we discuss the use of unitary circuits for the representation of standard families of dyadic wavelets (including Daubechies wavelets, coiflets and symlets), and then explore use of unitary circuits for the design of novel wavelet families (including symmetric multiwavelets of dilation factor $m = 3$ and $m = 4$, symmetric multiwavelets, boundary wavelets, and a new family of symmetric biorthogonal wavelets).

This paper is organized as follows. Firstly in Sect. II we introduce our notion of multi-scale unitary circuits, which follow as the classical analogue of MERA quantum circuits. Then in Sect. III we discuss the representation of discrete, orthogonal, dyadic wavelet transformations as unitary circuits. This includes providing the explicit form of the circuit representation for Daubechies wavelets, coiflets and symlets, as well as an algorithm for obtaining the circuit representation of arbitrary dyadic wavelets. In Sect. IV we explore the use of generalized unitary circuits in the design of novel WTs, including, in Sect. IV A families of symmetric dilation factor $m = 3$ wavelets, in Sect. IV B a family of symmetric multiwavelets, in Sect. IV C a family of symmetric dilation factor $m = 4$ wavelets, in Sect. IV D a construction of boundary wavelets, and in Sect. IV E a family of symmetric biorthogonal wavelets. Finally, conclusions and discussion are presented in Sect. V.

II. UNITARY CIRCUITS

In this section we define our notions of binary and multi-scale unitary circuits, which are the analogue of the MERA circuits[15] used for representing quantum many-body wavefunctions. First we consider a 1-parameter family of 2×2 unitary matrices $u(\theta_k)$, with the free parameter $\theta_k \in (-\pi, \pi]$, which is defined

$$u(\theta_k) \equiv \begin{bmatrix} \cos(\theta_k) & \sin(\theta_k) \\ -\sin(\theta_k) & \cos(\theta_k) \end{bmatrix},$$

$$= \cos(\theta_k) \begin{bmatrix} 1 & t_k \\ -t_k & 1 \end{bmatrix}, \quad (1)$$

where t_k is short for $\tan(\theta_k)$. Now let \mathcal{U} be a $2M \times 2M$ unitary matrix for integer M . We say \mathcal{U} is a binary unitary circuit of depth N if it can be written as a product of matrices U_k ,

$$\mathcal{U} = U_N \times U_{N-1} \times \dots \times U_2 \times U_1. \quad (2)$$

where each U_k is a $2M \times 2M$ unitary matrix that is the direct sum of M neighboring 2×2 unitary matrices $u(\theta_k)$ (alternating between odd-even and even-odd placement with each layer), i.e. such that

$$U_k \equiv \bigoplus_{r \text{ odd}} u_{[r, r+1]}(\theta_k), \quad (3)$$

for k odd, and with the direct sum over even r sites for k even, see also Fig. 1(a-b) for a diagrammatic representation.

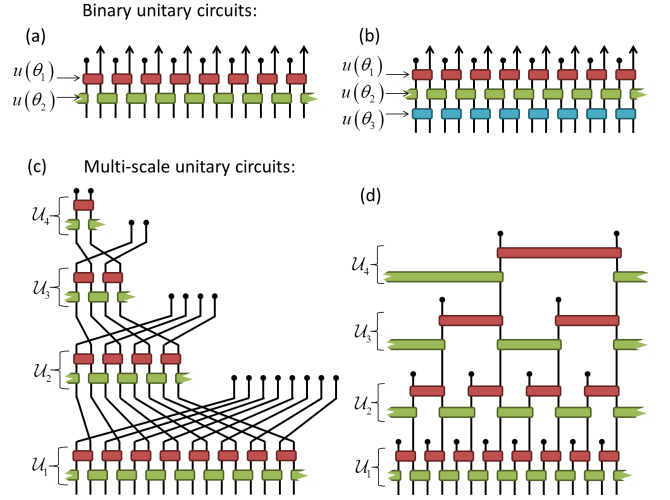


FIG. 1. (a) Depiction of a depth $N = 2$ binary unitary circuit, built from 2×2 unitary gates u , see Eq. 1, with angles $\{\theta_1, \theta_2\}$. (b) Depth $N = 3$ binary unitary circuit parameterized by angles $\{\theta_1, \theta_2, \theta_3\}$. (c) Multi-scale unitary circuit formed from composition of $N = 2$ binary unitary circuits, see also Eq. 4. (d) Alternative representation of the same multi-scale circuit from (c).

A multi-scale circuit, representing a matrix of dimension $2^T \times 2^T$ for positive integer T , can be formed from composition of T binary unitary circuits,

$$\mathcal{U}_1 \circ \mathcal{U}_2 \circ \dots \circ \mathcal{U}_T. \quad (4)$$

Here each \mathcal{U}_k is a binary unitary circuit of linear dimension 2^{T-k+1} and the composition is such that \mathcal{U}_k acts only on the even index sites of the previous \mathcal{U}_{k-1} , see also Fig. 1(c-d).

III. WAVELETS AND UNITARY CIRCUITS

In this section we describe how discrete WTs can be represented as unitary circuits, first in Sect. III A recalling basic properties of wavelets [8], before next in Sect. III B providing a specific example of the circuit representation of the D4 Daubechies wavelet, and finally in Sect. III C providing an algorithm for constructing the circuit representation of arbitrary dyadic orthogonal wavelets.

A. Basic properties of orthogonal wavelets

Here we recall the fundamentals of compact, dyadic (i.e. dilation factor $m = 2$), orthogonal wavelets. We seek to construct a set of wavelet functions ψ_z for $z = [1, 2, \dots]$ on a $1D$ lattice of sites, where z denotes the scale over which the function has non-zero support, such that wavelet ψ_z has a compact support of $O(2^z)$ sites. Additionally, we require that wavelets at different scales should be mutually orthogonal, and wavelets at the same

scale should be orthogonal under translations of $x = n2^z$ sites for integer n . The construction of wavelets that fulfill these properties is facilitated by first introducing the set of *scaling functions*, which we denote ϕ_z for $z = [1, 2, \dots]$, where z again denotes scale. The scaling functions are defined recursively through the *refinement equation* [9],

$$\phi_{z+1}(x) = \sum_{r=1}^{2N} h_r \phi_z(2x - r), \quad (5)$$

where $\mathbf{h} = [h_1, h_2, \dots, h_{2N}]$ is called the *scaling sequence*, with N the order of the wavelet transform. Note that the scaling function at smallest scale $z = 1$ is defined directly from the scaling sequence, $\phi_1(x) \equiv h_r \delta_{x,r}$, with $\delta_{i,j}$ the Kronecker delta function. A necessary condition for a scaling sequence \mathbf{h} to generate orthogonal wavelets is that it is orthogonal to itself under shifts by an even number of coefficients,

$$\sum_{r=1}^{2N-2m} h_r h_{r+2m} = \delta_{m,0}. \quad (6)$$

For dyadic wavelets, the wavelet sequence $\mathbf{g} = [g_1, g_2, \dots, g_{2N}]$ is defined from the scaling sequence \mathbf{h} by reversing the order of elements and introducing an alternating minus sign,

$$g_r = (-1)^{r+1} h_{2N-r+1}. \quad (7)$$

Notice that the wavelet sequence \mathbf{g} is, by construction, orthogonal to the scaling sequence \mathbf{h} from which it is derived. The wavelets ψ_z can now be defined from the scaling functions; specifically the wavelet ψ_{z+1} at scale $z+1$ is given from linear combinations of translations of scaling functions ϕ_z at the previous scale,

$$\psi_{z+1}(x) = \sum_{r=1}^{2N} g_r \phi_z(2x - r). \quad (8)$$

Following this recipe, any scaling sequence \mathbf{h} that satisfies the orthogonality constraints of Eq. 6 can be applied to generate a set of wavelet functions ψ_z for $z = [1, 2, \dots]$, which can be shown to form a complete and orthogonal basis for the 1D lattice.

In order to realize a wavelet transform that resolves high/low frequencies at each scale additional constraints are imposed on the wavelet sequence $\mathbf{g} = [g_1, g_2, \dots, g_{2N}]$, where the specific constraints may depend on the family of wavelets under consideration. For Daubechies wavelets with scaling sequence of $2N$ coefficients, denoted D2N wavelets, it is imposed that the first N moments of the wavelet sequence should vanish, i.e. that

$$\sum_{r=1}^{2N} (r^\alpha g_r) = 0, \quad (9)$$

for $\alpha = [0, 1, \dots, N-1]$.

B. Circuit representation of Daubechies D4 wavelets

We now provide an example of how the Daubechies D4 wavelets, which are characterized by the scaling sequence $\mathbf{h} \approx [0.48296, 0.83651, 0.22414, -0.12940]$, can be encoded as a binary unitary circuit \mathcal{U} of depth $N = 2$. More precisely, we show that the angles $\{\theta_1, \theta_2\}$ that define the circuit \mathcal{U} can be chosen such that the scaling sequence \mathbf{h} of the D4 wavelets is reproduced when transforming the unit vector $\mathbb{1}_r$ on any odd site r ,

$$\mathbf{h} = \langle \mathcal{U} \times \mathbb{1}_r \rangle, \quad (10)$$

where the brackets indicate that we only take the part of the vector with non-zero support, and ‘ \times ’ indicates standard matrix multiplication. Only a few of the local unitary u gates from \mathcal{U} contribute to this non-zero support, see also Fig. 2, such that Eq. 10 may be equivalently expressed as,

$$\mathbf{h} = (u_2 \oplus u_2) \times (1 \oplus u_1 \oplus 1) \times [0, 0, 1, 0, 0]^\dagger, \quad (11)$$

with ‘ \oplus ’ representing the direct sum. This expression can be evaluated in terms of the tangent angles t_1 and t_2 , see Eq. 1, that parameterize the local unitary matrices $u(\theta_1)$ and $u(\theta_2)$ respectively,

$$\begin{aligned} \begin{bmatrix} h_1 \\ h_2 \\ h_3 \\ h_4 \end{bmatrix} &= \begin{bmatrix} 1 & t_2 & 0 & 0 \\ -t_2 & 1 & 0 & 0 \\ 0 & 0 & 1 & t_2 \\ 0 & 0 & -t_2 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & t_1 & 0 \\ 0 & -t_1 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \end{bmatrix} \\ &= \begin{bmatrix} t_1 t_2 \\ t_1 \\ 1 \\ -t_2 \end{bmatrix}. \end{aligned} \quad (12)$$

Note that, for simplicity, we have neglected an overall normalization factor from the $\cos(\theta_k)$ contributions in Eq. 1. Similarly the wavelet sequence \mathbf{g} , which follows from transforming the unit vector $\mathbb{1}_r$ on any even site r , is given as,

$$\mathbf{g} = (u_2 \oplus u_2) \times (1 \oplus u_1 \oplus 1) \times [0, 1, 0, 0, 0]^\dagger, \quad (13)$$

which evaluates to,

$$\begin{bmatrix} g_1 \\ g_2 \\ g_3 \\ g_4 \end{bmatrix} = \begin{bmatrix} t_2 \\ 1 \\ -t_1 \\ t_1 t_2 \end{bmatrix}. \quad (14)$$

Notice that \mathbf{h} and \mathbf{g} satisfy the relation between wavelet and scaling sequences prescribed in Eq. 7 for any choice of the angles $\{\theta_1, \theta_2\}$. Substituting this parameterization for \mathbf{g} into Eq. 9 for moments $\alpha = \{0, 1\}$ gives,

$$\begin{aligned} 1 - t_1 + t_2 + t_1 t_2 &= 0, \\ 2 - 3t_1 + t_2 + 4t_1 t_2 &= 0. \end{aligned} \quad (15)$$

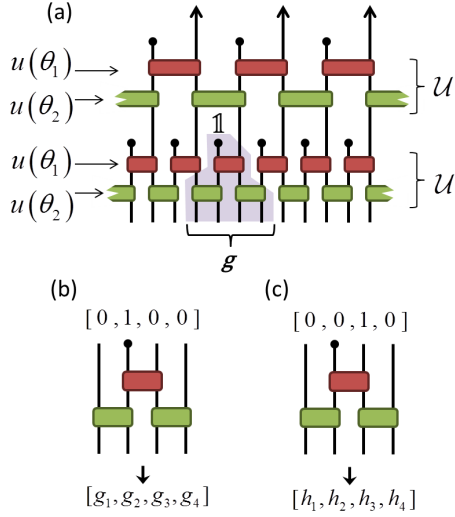


FIG. 2. (a) A multi-scale circuit formed from a binary circuit of depth $N = 2$. The wavelet coefficient sequence \mathbf{g} , obtained by transforming the unit vector $\mathbb{1}$, is depicted. (b) The wavelet sequence $\mathbf{g} = [g_1, g_2, g_3, g_4]$ is obtained by transforming the unit vector $\mathbb{1}_r$, with r even (corresponding to an index that terminates), through the binary circuit, see also Eq. 14. (c) The scaling sequence $\mathbf{h} = [h_1, h_2, h_3, h_4]$ is obtained by transforming the unit vector $\mathbb{1}_r$, with r odd (corresponding to an index that would connect with the next layer of the multi-scale circuit), through the binary circuit, see also Eq. 12.

These equations are satisfied for the tangent angles,

$$t_1 = 2 + \sqrt{3}, \quad t_2 = \frac{1}{\sqrt{3}}, \quad (16)$$

which gives the angles that parameterize the unitary circuit,

$$\theta_1 = \frac{5\pi}{12}, \quad \theta_2 = \frac{\pi}{6}, \quad (17)$$

Substituting these values in Eqs. 12 and 14 for scaling and wavelet sequences (when normalized to unity) yields,

$$\mathbf{h} \approx \begin{bmatrix} 0.48296 \\ 0.83651 \\ 0.22414 \\ -0.12940 \end{bmatrix}, \quad \mathbf{g} \approx \begin{bmatrix} 0.12940 \\ 0.22414 \\ -0.83651 \\ 0.48296 \end{bmatrix}, \quad (18)$$

which equates to the known D4 sequences [3].

C. Circuit representation of generic dyadic wavelets

We now describe how to construct the unitary circuit representation for generic (compact, orthogonal, dyadic) wavelet transformations. Let \mathcal{U} be a binary unitary circuit of depth N , which is parameterized by the set of angles $\{\theta_1, \theta_2, \dots, \theta_N\}$. We associate scaling \mathbf{h} and wavelet

\mathbf{g} sequences of $2N$ coefficients to the (non-zero support of the) transformation of the unit vector $\mathbb{1}_r$ on odd or even sites,

$$\mathbf{h} = \langle \mathcal{U} \times \mathbb{1}_r \rangle, \quad r \text{ odd} \quad (19)$$

$$\mathbf{g} = \langle \mathcal{U} \times \mathbb{1}_r \rangle, \quad r \text{ even}. \quad (20)$$

We shall argue the following:

1. Any scaling \mathbf{h} and wavelet \mathbf{g} sequences of $2N$ coefficients (that satisfy the orthogonality constraints of Eq. 6 and are related as in Eq. 7) can be uniquely encoded as a depth N binary unitary circuit (up to an overall normalization).
2. Any orthogonal, dyadic WT can be represented as a multi-scale unitary circuit, as described in Eq. 4 and depicted in Fig. 1, which is formed from composition of the appropriate binary unitary circuit that encodes the scaling and wavelet sequences.

Notice it follows trivially that the scaling \mathbf{h} coefficient sequences from unitary circuits satisfy the orthogonality constraints of Eq. 6, as shifts of the scaling sequence correspond to different columns of the unitary matrix \mathcal{U} . In Sect. III C 1 we offer a proof that \mathbf{h} and \mathbf{g} satisfy the relation of Eq. 7, while in Sect. III C 2 we describe an algorithm that, for any scaling sequence \mathbf{h} , generates the set of angles $\{\theta_1, \theta_2, \dots, \theta_N\}$ that parameterizes a depth N unitary circuit that encodes the sequence. Together these two results prove statement 1 above. Statement 2 then follows easily, as the composition of binary unitary circuits, described in Eq. 4 and depicted in Fig. 1(c), is clearly seen to be equivalent to the refinement equation of Eq. 5.

1. Relation between scaling and wavelet sequences

Here we offer a proof that scaling \mathbf{h} and wavelet \mathbf{g} sequences from unitary circuits always satisfy the relation of Eq. 7. We begin by defining the *spatial reflection* operator \mathcal{R} which reverses the order of both rows and columns of a matrix, i.e if for a given $N \times N$ matrix A we have that $\tilde{A} \equiv \mathcal{R}(A)$ then the matrix elements of A and \tilde{A} are related as

$$\tilde{A}_{i,j} = A_{N-i+1, N-j+1}. \quad (21)$$

Notice that spatial reflection of a 2×2 unitary u from Eq. 1 changes the sign of the angle θ ,

$$\mathcal{R}(u(\theta)) = u(-\theta). \quad (22)$$

It follows that, if \mathcal{U} is a binary unitary circuit parameterized by angles $\{\theta_1, \theta_2, \dots, \theta_N\}$, then its spatial reflection $\tilde{\mathcal{U}} \equiv \mathcal{R}(\mathcal{U})$ is a binary unitary circuit with opposite sign angles $\{-\theta_1, -\theta_2, \dots, -\theta_N\}$. Notice that spatial reflection of circuit \mathcal{U} into $\tilde{\mathcal{U}}$ has exchanged the role of the scaling and wavelet sequences, such that if

$\mathbf{g} = [g_1, g_2, \dots, g_{2N}]$ is the wavelet sequence of \mathcal{U} and $\tilde{\mathbf{h}} = [\tilde{h}_1, \tilde{h}_2, \dots, \tilde{h}_{2N}]$ is the scaling sequence of $\tilde{\mathcal{U}}$, then

$$g_r = \tilde{h}_{2N-r+1}, \quad (23)$$

see also Fig. 3(a). Thus in order to demonstrate the relation between \mathbf{h} and \mathbf{g} of Eq. 7, it suffices to show that the elements of \mathbf{h} and $\tilde{\mathbf{h}}$ are related with an alternating negative sign,

$$\tilde{h}_r = (-1)^r h_r, \quad (24)$$

see also Fig. 3(b), which we now prove.

Consider the factorization of the circuit into its constituent layers,

$$\mathcal{U} = U_N \times \dots \times U_2 \times U_1, \quad (25)$$

where each U_k is a function of some θ_k . Let $\mathbf{s} = [s_1, s_2, \dots, s_{2M}]$ and $\tilde{\mathbf{s}} = [\tilde{s}_1, \tilde{s}_2, \dots, \tilde{s}_{2M}]$ be vectors of length $2M$ for integer M , and assume $\tilde{s}_r = (-1)^r s_r$. Define \mathbf{s}' as given by the transform \mathbf{s} by circuit layer $U(\theta)$,

$$\mathbf{s}' \equiv U(\theta) \times \mathbf{s} \quad (26)$$

and $\tilde{\mathbf{s}}'$ as given by the transform of $\tilde{\mathbf{s}}$ by a layer $U(-\theta)$ of opposite sign,

$$\tilde{\mathbf{s}}' \equiv U(-\theta) \times \tilde{\mathbf{s}}. \quad (27)$$

If it can be shown that $\tilde{s}'_r = (-1)^r s'_r$, then Eq. 24 follows from recursion over all layers U_k of the binary circuit \mathcal{U} ; in order to show this we evaluate elements of \mathbf{s}' from Eq. 26,

$$\begin{aligned} \begin{bmatrix} s'_r \\ s'_{r+1} \end{bmatrix} &\equiv \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} s_r \\ s_{r+1} \end{bmatrix} \\ &= \begin{bmatrix} s_r \cos(\theta) + s_{r+1} \sin(\theta) \\ -s_r \sin(\theta) + s_{r+1} \cos(\theta) \end{bmatrix}, \end{aligned} \quad (28)$$

and similarly evaluate elements $\tilde{\mathbf{s}}'$ from Eq. 27,

$$\begin{aligned} \begin{bmatrix} \tilde{s}'_r \\ \tilde{s}'_{r+1} \end{bmatrix} &\equiv \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} \tilde{s}_r \\ \tilde{s}_{r+1} \end{bmatrix} \\ &= \begin{bmatrix} \tilde{s}_r \cos(\theta) - \tilde{s}_{r+1} \sin(\theta) \\ \tilde{s}_r \sin(\theta) + \tilde{s}_{r+1} \cos(\theta) \end{bmatrix} \\ &= \begin{bmatrix} -s_r \cos(\theta) - s_{r+1} \sin(\theta) \\ -s_r \sin(\theta) + s_{r+1} \cos(\theta) \end{bmatrix} \\ &= \begin{bmatrix} -s'_r \\ s'_{r+1} \end{bmatrix}, \end{aligned} \quad (29)$$

from which the desired result is observed. Thus we conclude that the scaling \mathbf{h} and wavelet \mathbf{g} sequences from a binary unitary circuit are always related as per Eq. 7.

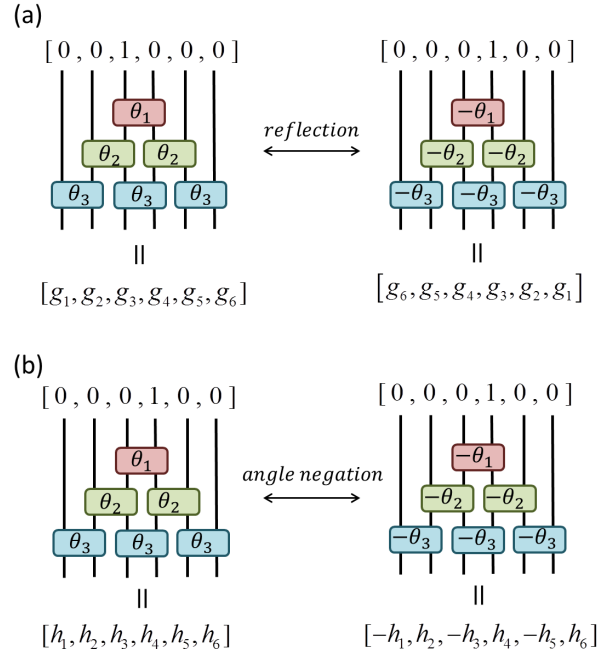


FIG. 3. (a) The wavelet sequence \mathbf{g} associated to a depth $N = 3$ binary circuit. A spatial reflection of the circuit exchanges the positions of the wavelet \mathbf{g} and \mathbf{h} scaling sequences, and negates the angles θ of the local unitary gates. (b) The scaling sequence \mathbf{h} associated to a depth $N = 3$ binary circuit. After negation of the angles θ , the elements of the new scaling sequence $\tilde{\mathbf{h}}$ relate to the previous as $\tilde{h}_r = (-1)^{r+1} h_r$. Together (a) and (b) imply the relation between wavelet \mathbf{g} and scaling \mathbf{h} sequences of Eq. 7.

2. Circuit construction algorithm

Given a discrete, orthogonal WT described by the scaling sequence $\mathbf{h} = [h_1, h_2, \dots, h_{2N}]$ of $2N$ coefficients, we now describe an algorithm to encode the sequence as a depth N binary unitary circuit. More precisely, we describe how the angles $\{\theta_1, \theta_2, \dots, \theta_N\}$ defining the circuit can be uniquely chosen such that the scaling sequence is mapped to a unit vector $\mathbb{1}_r$ under transformation by the circuit,

$$\mathbf{h}^\dagger \times \mathcal{U} = (\mathbb{1}_r)^\dagger, \quad (30)$$

in accordance with the definition of Eq. 19. Recall that the binary circuit decomposes into N layers, $\mathcal{U} = U_N U_{N-1} \dots U_1$, where each layer U_k is the direct sum of a 2×2 unitary matrices $u(\theta_k)$. Let \mathbf{h}' be the scaling sequence after transforming by the bottom layer U_N of the unitary circuit,

$$(\mathbf{h}')^\dagger \equiv \mathbf{h}^\dagger \times U_N, \quad (31)$$

We now propose that the free angle θ_N of unitary $u(\theta_N)$ should be chosen as,

$$\theta = \begin{cases} \text{(i)} & \arctan\left(\frac{h_1}{h_2}\right), & h_2 \neq 0 \\ \text{(ii)} & \arctan\left(\frac{-h_{2N}}{h_{2N-1}}\right), & h_2 = 0, h_{2N-1} \neq 0 \\ \text{(iii)} & \pi/2, & h_2 = h_{2N-1} = 0. \end{cases} \quad (32)$$

Under this choice the first element of the transformed scaling sequence \mathbf{h}' is zero,

$$h'_1 = h_1 \cos(\theta) - h_2 \sin(\theta) = 0. \quad (33)$$

for all three possibilities (i-iii) from Eq. 32. To understand this in the second instance (ii) notice that the orthogonality constraints of Eq. 6 impose,

$$h_1 h_{2N-1} + h_2 h_{2N} = 0, \quad (34)$$

which implies that $h_1 = 0$ given that $h_{2N-1} \neq 0$. Similarly, the trailing $(2N)^{\text{th}}$ element of \mathbf{h}' is also mapped to zero,

$$h'_{2N} = h_{2N-1} \sin(\theta) + h_{2N} \cos(\theta) = 0. \quad (35)$$

In instances (ii) and (iii) from Eq. 32 this follows trivially, whereas in the first instance (i) this can be understood by substituting the orthogonality constraint of Eq. 6 to give,

$$\begin{aligned} h'_{2N} &= h_{2N} (-h_2/h_1 \sin(\theta) + \cos(\theta)), \\ &= (h_{2N} h'_1)/h_1 = 0. \end{aligned} \quad (36)$$

Thus we have demonstrated that under the choice of angle θ from Eq. 32 the scaling sequence \mathbf{h} of $2N$ coefficients is mapped under U_N to a new sequence \mathbf{h}' of $2N-2$ coefficients (where the first and last elements of \mathbf{h}' , which were shown to be zero, have been dropped). It can also easily be seen that the orthogonality constraints on \mathbf{h} , see Eq. 6, map to an equivalent set of constraints for the new sequence \mathbf{h}' . The set of angles $\{\theta_N, \theta_{N-1}, \dots, \theta_2, \theta_1\}$ is obtained by iterating this procedure a total of $N-1$ times, i.e. for unitary layers $\{U_N, U_{N-1}, \dots, U_2\}$, which then maps the initial scaling sequence \mathbf{h} of $2N$ coefficients into a sequence of length two denoted $\mathbf{h}^f = [h_1^f, h_2^f]$. At this stage, the angle θ_1 associated to the top level U_1 is fixed at,

$$\theta_1 = \tan^{-1}(h_1^f/h_2^f), \quad (37)$$

such that \mathbf{h}^f is mapped to a sequence with only a single non-zero element, indicating that the scaling sequence is encoded in the binary unitary circuit.

Employing this algorithm we generate the sets of angles that describe the Daubechies wavelets D2N for $N = \{1, 2, \dots, 10\}$, see Tab. I, the symlets of $2N$ coefficients for $N = \{1, 2, \dots, 10\}$, see Tab. II, and the coiflets of $2N$ coefficients for $N = \{3, 6, 9, 12, 15\}$, see Tab. III. Notice that clear patterns are evident in the angles θ between different orders N of wavelets in each of the families, see also Fig. 4.

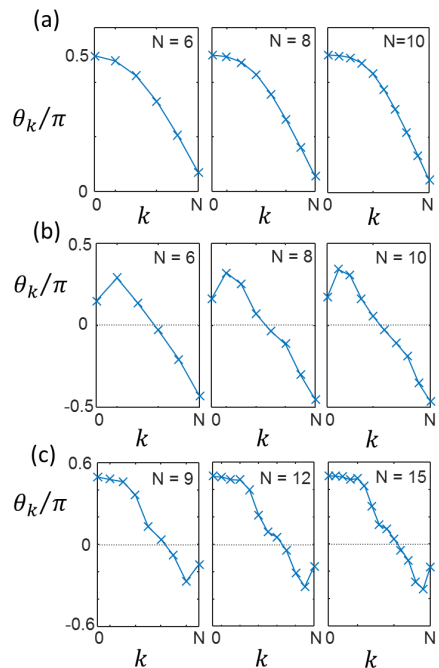


FIG. 4. Plots of the angles θ_k that parameterize the circuit representations of (a) the D2N Daubechies wavelets for $N = \{6, 8, 10\}$, (b) the symlets of $2N$ coefficients for $N = \{6, 8, 10\}$, and (c) the coiflets of $2N$ coefficients for $N = \{9, 12, 15\}$.

IV. CIRCUIT CONSTRUCTIONS OF NOVEL WAVELETS

In the remainder of this manuscript we discuss the use of generalized unitary circuits for the design and realization of novel wavelet families. This includes families of (dilation factor $m = 3$) symmetric wavelets in Sect. IV A, symmetric multiwavelets in Sect. IV B, a family of (dilation factor $m = 4$) symmetric wavelets in Sect. IV C, boundary wavelets in Sect. IV D, and symmetric biorthogonal wavelets in Sect. IV E. Many of the generalized circuits considered are direct analogues of circuits considered previously in the context of MERA for quantum many-body systems (for instance, of the reflection symmetric MERA considered in Refs. 20 and 21, of the MERA of different dilation factors considered in Refs. 18 and 25, and of the boundary MERA considered in Refs. 26 and 27).

A. Dilation $m = 3$ symmetric wavelets

An often desirable characteristic of wavelets is symmetry (or antisymmetry) under spatial reflections. However it is known that the only compactly supported orthogonal wavelet basis of dilation factor $m = 2$ that consists of symmetric (or antisymmetric) functions is the trivial Haar basis[3, 4]. One solution to this problem is to use a larger dilation factor $m > 2$, which results in a scheme

	D2	D4	D6	D8	D10	D12	D14	D16	D18	D20
θ_1/π	1/4	5/12	0.466419	0.485368	0.493368	0.496925	0.498553	0.499312	0.499671	0.499841
θ_2/π	-	1/6	0.340895	0.419242	0.457854	0.477754	0.488217	0.493760	0.496701	0.498260
θ_3/π	-	-	0.124476	0.283112	0.372126	0.424117	0.455055	0.473548	0.484560	0.491068
θ_4/π	-	-	-	0.099238	0.240141	0.330420	0.389528	0.428559	0.454286	0.471103
θ_5/π	-	-	-	-	0.082499	0.207731	0.295133	0.357027	0.401092	0.432370
θ_6/π	-	-	-	-	-	0.070599	0.182705	0.265668	0.327768	0.374473
θ_7/π	-	-	-	-	-	-	0.061708	0.162913	0.241041	0.301941
θ_8/π	-	-	-	-	-	-	-	0.054813	0.146919	0.220319
θ_9/π	-	-	-	-	-	-	-	-	0.049309	0.133750
θ_{10}/π	-	-	-	-	-	-	-	-	-	0.044815

TABLE I. Set of angles θ that parameterize the depth N binary unitary circuit corresponding to the D2N Daubechies wavelets.

	$N = 1$	$N = 2$	$N = 3$	$N = 4$	$N = 5$	$N = 6$	$N = 7$	$N = 8$	$N = 9$	$N = 10$
θ_1/π	1/4	5/12	0.466419	0.128000	0.197549	0.149210	0.418681	0.162192	0.207549	0.171178
θ_2/π	-	1/6	0.340895	0.213974	-0.086984	0.289866	-0.195828	0.323040	-0.481080	0.343162
θ_3/π	-	-	0.124476	-0.045343	0.279718	0.138289	0.068910	0.252744	-0.018742	0.308034
θ_4/π	-	-	-	-0.381317	0.076487	-0.028270	0.498795	0.071840	0.380963	0.163525
θ_5/π	-	-	-	-	-0.237764	-0.204970	-0.277830	-0.032859	0.331334	0.059282
θ_6/π	-	-	-	-	-	-0.429066	0.038275	-0.112982	0.180695	-0.027548
θ_7/π	-	-	-	-	-	-	0.381482	-0.299591	0.086208	-0.104053
θ_8/π	-	-	-	-	-	-	-	-0.449411	-0.091644	-0.185998
θ_9/π	-	-	-	-	-	-	-	-	-0.367415	-0.351975
θ_{10}/π	-	-	-	-	-	-	-	-	-	-0.460675

TABLE II. Set of angles θ that parameterize the depth N binary unitary circuit corresponding to the symlets of $2N$ coefficients.

	$N = 3$	$N = 6$	$N = 9$	$N = 12$	$N = 15$
θ_1/π	0.432513	0.486012	0.497096	0.499363	0.499855
θ_2/π	0.115026	0.449082	0.478861	0.494102	0.498385
θ_3/π	-0.067486	0.293308	0.462006	0.474920	0.491529
θ_4/π	-	0.036930	0.365035	0.471844	0.472624
θ_5/π	-	-0.163110	0.132236	0.401463	0.479637
θ_6/π	-	-0.119802	0.040847	0.216145	0.423857
θ_7/π	-	-	-0.080093	0.091539	0.274343
θ_8/π	-	-	-0.267867	0.053920	0.139303
θ_9/π	-	-	-0.144368	-0.041439	0.111993
θ_{10}/π	-	-	-	-0.209282	0.038183
θ_{11}/π	-	-	-	-0.308590	-0.041666
θ_{12}/π	-	-	-	-0.159473	-0.122667
θ_{13}/π	-	-	-	-	-0.278205
θ_{14}/π	-	-	-	-	-0.332208
θ_{15}/π	-	-	-	-	-0.170007

TABLE III. Set of angles θ that parameterize the depth N binary unitary circuit corresponding to the coiflets of $2N$ coefficients.

with one scaling and $(m-1)$ wavelet functions. Constructions of wavelets with larger dilation factors have been studied extensively in previous works, see for instance Refs. 28–31. In this Section we consider the design of novel symmetric (and/or antisymmetric) wavelets with dilation factor $m = 3$.

In the context of MERA quantum circuits, reflection symmetry (and, more generally, other spatial symmetries) are imposed by requiring that the individual unitary gates that comprise the circuit satisfy the symmetry[20, 21]. Here we follow a similar strategy, and construct reflection symmetric wavelets using unitary circuits where all of the unitary matrices that comprise the circuit are individually symmetric under spatial reflections. For 2×2 unitary matrices, there is only a single non-trivial instance of a matrix, which we denote u_{sw} , that is invariant under reflections \mathcal{R} (as defined in Eq. 21),

$$u_{\text{sw}} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \quad (38)$$

which simply enacts a swap of elements on a length 2 vector. For 3×3 unitary matrices, a 1-parameter family of reflection symmetric matrices $v(\theta)$ is obtained by exponentiating the most general instance of a real skew-hermitian matrix that is also reflection symmetric,

$$v(\theta) = \exp \left(\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & \theta & 0 \\ -\theta & 0 & -\theta \\ 0 & \theta & 0 \end{bmatrix} \right), \quad (39)$$

which evaluates to,

$$v(\theta) = \frac{1}{2} \begin{bmatrix} \cos(\theta) + 1 & \sqrt{2} \sin(\theta) & \cos(\theta) - 1 \\ -\sqrt{2} \sin(\theta) & 2 \cos(\theta) & -\sqrt{2} \sin(\theta) \\ \cos(\theta) - 1 & \sqrt{2} \sin(\theta) & \cos(\theta) + 1 \end{bmatrix}. \quad (40)$$

We now describe how to build a unitary circuit from these 3×3 reflection symmetric matrices $v(\theta)$ in conjunction with the swap gate u_{sw} , that will subsequently be used to parameterize a family of symmetric wavelet transforms with dilation factor $m = 3$.

1. Ternary unitary circuits

Let \mathcal{V} be a $3M \times 3M$ matrix for integer M ; we say that \mathcal{V} is a *ternary unitary circuit* of depth N if it can be decomposed as,

$$\mathcal{V} = V_N U_{\text{sw}} V_{N-1} U_{\text{sw}} \dots V_2 U_{\text{sw}} V_1 U_{\pm}, \quad (41)$$

see also the circuit diagram of Fig. 5. Here each of the N sublayers V_k is a direct sum of M matrices $v(\theta_k)$ from Eq. 40,

$$V_k = \dots \oplus v(\theta_k) \oplus v(\theta_k) \oplus v(\theta_k) \oplus \dots, \quad (42)$$

Ternary unitary circuits:

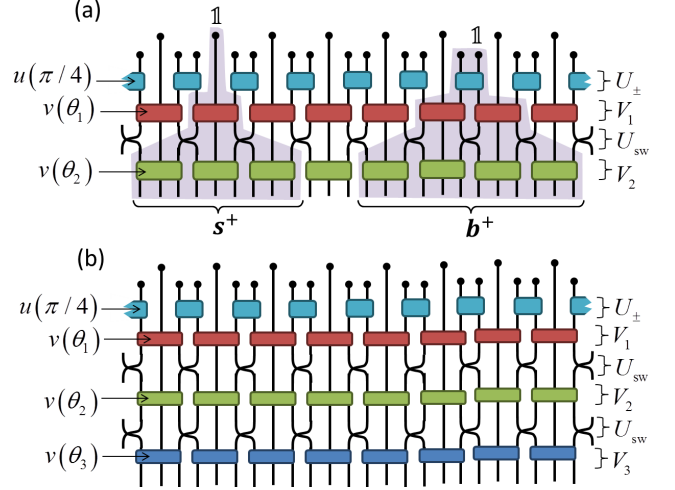


FIG. 5. (a) A depth $N = 2$ ternary unitary circuit. Layers V_k are composed of a direct sum of 3×3 reflection symmetric matrices v of Eq.40, which are interspersed with layers U_{sw} composed of two site swap gates u_{sw} of Eq.38 (depicted as the crossing of wires). The top layer of the circuit U_{\pm} is composed of 2×2 matrices u of Eq.1 with angle $\theta = \pi/4$, which creates reflection symmetric / antisymmetric outputs from input unit vectors. Transforming a unit vector $\mathbb{1}$ located at the central site of a v matrix gives (site-centered) symmetric sequence \mathbf{s}^+ , while a unit vector on the right site of a u matrix gives (edge-centered) symmetric sequence \mathbf{b}^+ and a unit vector on the left site of a u matrix gives (edge-centered) antisymmetric sequence \mathbf{b}^- (not shown). (b) A depth $N = 3$ ternary unitary circuit.

which are interspersed with sublayers U_{sw} consisting of direct sums of swap gates u_{sw} from Eq. 38,

$$U_{\text{sw}} = \dots \oplus u_{\text{sw}} \oplus \mathbb{I} \oplus u_{\text{sw}} \oplus \mathbb{I} \oplus u_{\text{sw}} \oplus \mathbb{I} \oplus \dots, \quad (43)$$

with \mathbb{I} the 1×1 identity. The ternary circuit \mathcal{V} includes a top sublayer U_{\pm} composed of 2×2 unitary gates $u(\pi/4)$ which are spaced by contributions of the identity,

$$U_{\pm} = \dots \oplus u(\pi/4) \oplus \mathbb{I} \oplus u(\pi/4) \oplus \mathbb{I} \oplus \dots \quad (44)$$

Notice that the ternary unitary circuit of depth N is fully parameterized by the set of angles $\{\theta_1, \theta_2, \dots, \theta_N\}$. There are three coefficient sequences associated to a ternary circuit (which corresponds to a three-channel filter bank), which we label $\{\mathbf{s}^+, \mathbf{b}^+, \mathbf{b}^-\}$. Each of the three sequences is obtained by transforming a unit vector $\mathbb{1}_r$ on different sites r with the ternary circuit \mathcal{V} ,

$$\langle \mathcal{V} \times \mathbb{1}_r \rangle = \begin{cases} \text{(i)} & \mathbf{s}^+, & r = 2, 5, 8, \dots \\ \text{(ii)} & \mathbf{b}^+, & r = 3, 6, 9, \dots \\ \text{(iii)} & \mathbf{b}^-, & r = 1, 4, 7, \dots \end{cases} \quad (45)$$

see also Fig. 5. The sequences possess the following properties:

- \mathbf{s}^+ is a site-centered symmetric sequence of (odd) length $6N-3$ elements (i.e. that is symmetric w.r.t. reflections about its central element)
- \mathbf{b}^+ is a edge-centered symmetric sequence of (even) length $6N$ elements (i.e. that is symmetric w.r.t. reflections centered between its two central elements)
- \mathbf{b}^- is a edge-centered antisymmetric sequence of (even) length $6N$ elements (i.e. that is antisymmetric w.r.t. reflections centered between its two central elements).

Similar to the construction applied to the binary unitary circuit in Sect. II, layers of the ternary circuit can be composed to form a multi-scale circuit,

$$\mathcal{V}_1 \circ \mathcal{V}_2 \circ \mathcal{V}_3 \circ \mathcal{V}_4 \circ \dots, \quad (46)$$

which encodes the dilation factor 3 discrete WT. Notice that there are two distinct ways of implementing this composition dependent on whether \mathbf{s}^+ or \mathbf{b}^+ is considered as the scaling sequence, which we refer to as the site-centered or edge-centered multi-scale circuits respectively, see also Fig. 6.

2. Example 1: dilation $m = 3$ wavelets with maximal vanishing moments

A depth N ternary unitary circuit offers a parameterization of exactly reflection symmetric and antisymmetric wavelets with N free parameters $\{\theta_1, \theta_2, \dots, \theta_N\}$. In this section we consider the family of wavelets that result from choosing these parameters to maximize the number of vanishing moments that the wavelets possess.

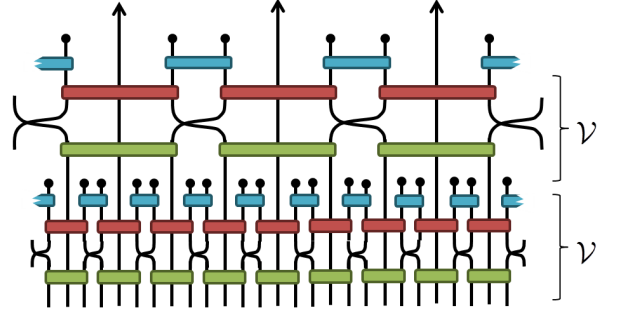
We use the site-centered form of the multi-scale circuit as depicted in Fig. 6(a), where sequence \mathbf{s}^+ is treated as the scaling function and \mathbf{b}^+ , \mathbf{b}^- are the wavelet sequences, and we optimize the angles θ_k such the wavelets have vanishing moments,

$$\sum_r (r^\alpha b_r^+) = 0, \quad \sum_r (r^\alpha b_r^-) = 0, \quad (47)$$

for $\alpha = [0, 1, 2, \dots]$. Notice that \mathbf{b}^+ is automatically orthogonal to odd α polynomials due to its symmetry, and similarly \mathbf{b}^- is automatically orthogonal to even α polynomials. Thus satisfying Eq. 47 for orders $\alpha = [0, 1, 2, \dots, N-1]$, i.e. such that the wavelets have N vanishing moments, requires N non-trivial constraints to be met.

The sets of angles $\{\theta_1, \theta_2, \dots, \theta_N\}$ that satisfy the vanishing moment criteria for circuit depths $N = 2, 4, 6$ are given in Tab. IV. These were obtained numerically using the standard Nelder-Mead algorithm to minimize the cost function given by the sum of the first N moments of the wavelet sequences. The resulting wavelets are depicted in Fig. 7. Interestingly, while the scaling functions

(a) Site-centered symmetric



(b) Edge-centered symmetric

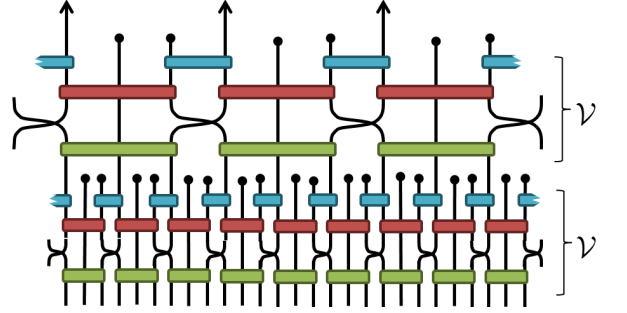


FIG. 6. Two different types of multi-scale circuit formed from composition of depth $N = 2$ ternary unitary circuits. (a) The site-centered multi-scale circuit is given when treating sequence \mathbf{s}^+ of Fig. 5 as the scaling function. (b) The edge-centered multi-scale circuit is given when treating sequence \mathbf{b}^+ of Fig. 5 as the scaling function. Both types of multiscale circuit describe orthogonal, dilation factor 3, discrete wavelet transforms with exactly symmetric / antisymmetric wavelets.

associated to these WTs appear similar to those obtained previously in Figs. 3 and 5 of Ref. 28, the wavelets themselves are seen to have much smaller effective support (i.e. the region over which the wavelets have non-vanishingly small amplitude is reduced), which suggests they may perform better in practical applications.

	$N = 2$	$N = 4$	$N = 6$
θ_1	0.275642799	0.595157579	0.756972477
θ_2	0.679673818	-0.840085482	-1.401172929
θ_3	-	-0.314805259	0.537202982
θ_4	-	1.515049781	0.264416395
θ_5	-	-	-1.007834534
θ_6	-	-	1.805732227

TABLE IV. Angles θ_k parameterizing the site-centered ternary circuits of depths $N = \{2, 4, 6\}$ such that the wavelets have N vanishing moments.

	\mathbf{s}^+	\mathbf{b}^+	\mathbf{b}^-
Type I	low freq. (scaling)	mid freq. (wavelet)	high freq. (wavelet)
Type II	mid freq. (wavelet)	low freq. (scaling)	high freq. (wavelet)
Type III	high freq. (wavelet)	low freq. (scaling)	mid freq. (wavelet)

TABLE V. Characterization of the three distinct possibilities of assigning a low/mid/high frequency range to the three coefficient sequences $\{\mathbf{s}^+, \mathbf{b}^+, \mathbf{b}^-\}$ of a ternary unitary circuit. Note that Type I wavelets correspond to the site-centered circuit as depicted in Fig. 6, while Types II-III correspond to the edge-centered circuit. Example wavelets of these types are presented in Fig. 8(a-c).

3. Example 2: dilation $m = 3$ wavelets with low/mid/high frequency components

Choosing the angles $\{\theta_1, \theta_2, \dots, \theta_N\}$ that parameterize the ternary circuit \mathcal{V} to maximize the vanishing moments of the wavelets, as per Sect. IV A 2, has several notable deficiencies. One of these deficiencies is that the symmetric and anti-symmetric wavelets seen in Fig. 7 are not well separated when resolved in frequency space; ideally we want the three-channel filter bank represented by circuit \mathcal{V} to possess well resolved low, mid, and high frequency components. A second deficiency is that the scaling functions in Fig. 7 still contain a significant high frequency component, which results in the corresponding wavelets not having a high degree of smoothness. In this Section we explore an alternative optimization criteria that resolves these deficiencies.

The alternative criteria we propose is that the circuit should be optimized such that some sequences $\mathbf{h} = [h_1, h_2, \dots]$ have vanishing moments at high frequencies,

$$\sum_r \left((-1)^r (r^\alpha) h_r \right) = 0. \quad (48)$$

A three-channel wavelet filter bank with well resolved low/mid/high frequencies can be achieved by requiring that the scaling function and *one* of the wavelets satisfy the (high frequency) orthogonality constraint of Eq. 48 for some $\alpha = [0, 1, \dots]$ (while also requiring that both wavelets satisfy the standard vanishing moment criteria of Eq. 9). Recall that the ternary unitary circuit has three associated sequences $\{\mathbf{s}^+, \mathbf{b}^+, \mathbf{b}^-\}$, as such there freedom as to how the sequences are associated to the low/mid/high frequency components (which also informs whether the bond-centered or edge-centered form of the ternary circuit is used, see Fig. 6). Specifically, there are three choices (which we call Types I-III) that are compatible with the symmetries of the sequences, see Tab. V.

In Tab. VI we present angles $\{\theta_1, \theta_2, \dots, \theta_6\}$ for ternary circuits of depth $N = 6$ for each of the wavelet

types I-III, which were again optimized numerically using Nelder-Mead minimization. The wavelet sequences were optimized to satisfy the (low frequency) orthogonality constraint of Eq. 9 for $\alpha = [0, 1, 2]$, while the scaling and mid-frequency wavelet sequences were simultaneously optimized to satisfy the (high frequency) orthogonality constraint of Eq. 48 for $\alpha = [0, 1, 2]$. Interesting to note is that the Type II wavelet has $\theta_2 = \theta_4 = \pi$ and $\theta_6 = 0$, which can be shown to imply that the sequence $\mathbf{b}^+ = [b_1^+, b_2^+, b_3^+, \dots]$ is strictly zero for all even indexed entries, i.e. $b_r^+ = 0$ for even r , which is compatible with its status as the mid-frequency wavelet. Furthermore, the final layer of $\theta_6 = 0$ gates could also be omitted, such that it could be regarded as a depth $N = 5$ ternary circuit that has an extra layer U_{sw} of swap gates on the bottom. Notice that the deficiencies observed in the previous class of scale factor 3 wavelets, Fig. 7, have been resolved; the new wavelets have high smoothness and are well separated into low/mid/high frequency components.

	Type I	Type II	Type III
θ_1	0.072130476	-0.261582176	0.072130476
θ_2	0.847695078	π	-0.847695078
θ_3	-0.576099009	0.107465734	-0.576099009
θ_4	-0.591746629	π	0.591746629
θ_5	0.673886987	-0.461363266	0.673886987
θ_6	0.529449713	0	-0.529449713

TABLE VI. Angles θ_k parameterizing depth $N = 6$ ternary unitary circuits which generate the wavelets depicted in Fig. 8.

B. Dilation $m = 2$ symmetric multi-wavelet transform

An alternative solution to form symmetric orthogonal wavelets, other than from increasing the dilation factor $m > 2$, is to use *multiwavelets*, which possess more than one distinct scaling function (see for instance Refs. 32–35). In this section we use the unitary circuit formalism to construct a family of dilation factor 2 multi-wavelets (noting that analogous constructions have previously been considered in the context of the MERA[18]) where the two distinct scaling functions are each exactly reflection symmetric, and the two distinct wavelet functions are reflections of one another.

1. Modified ternary unitary circuits

Let $\tilde{\mathcal{V}}$ be a $4M \times 4M$ matrix; we say that $\tilde{\mathcal{V}}$ is a depth N *modified ternary circuit* if it can be decomposed as a product of N layers,

$$\tilde{\mathcal{V}} = \tilde{V}_N \tilde{V}_{N-1} \dots \tilde{V}_2 \tilde{V}_1, \quad (49)$$

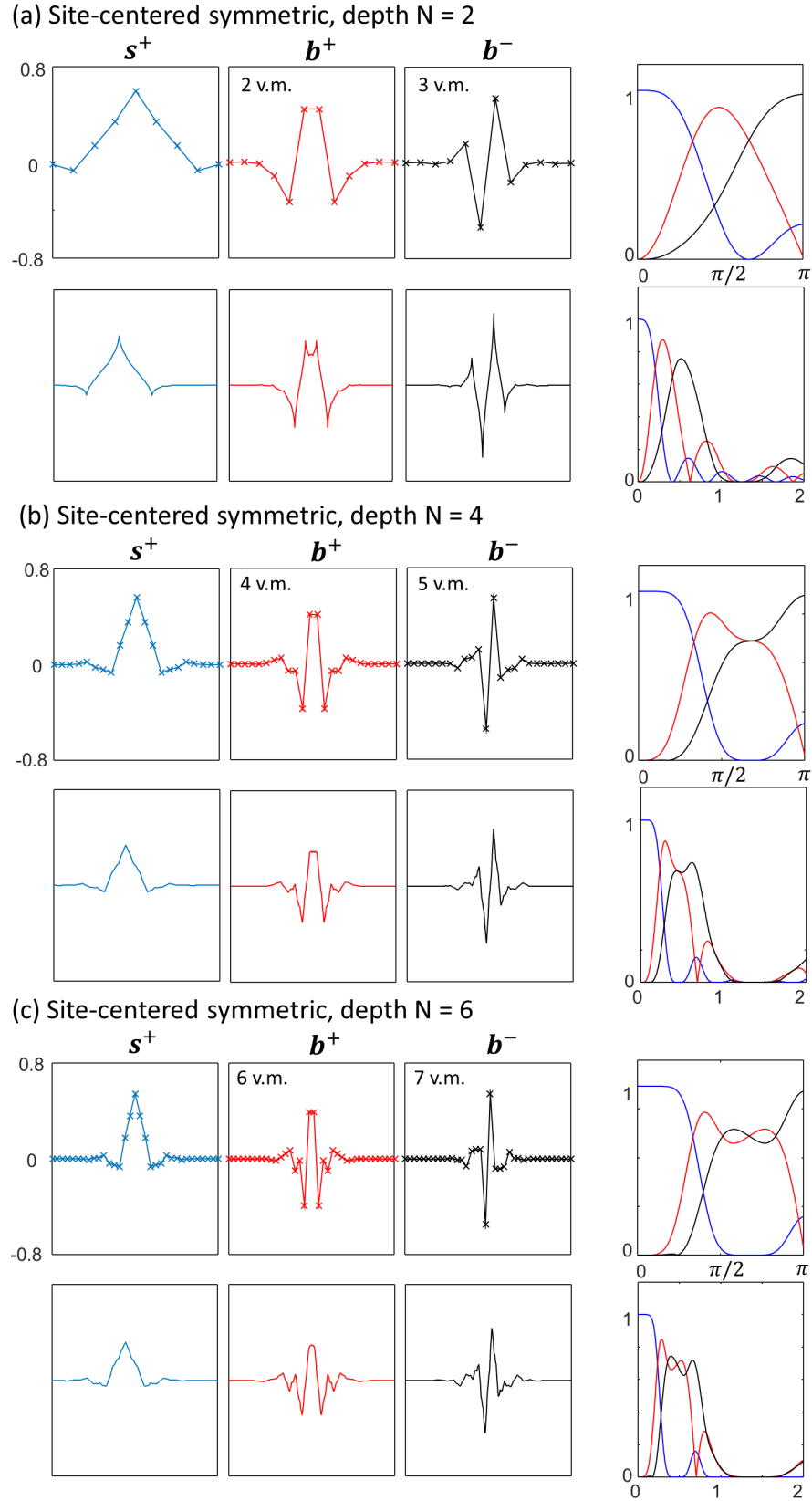


FIG. 7. Plots of the orthogonal wavelets given from site-centered symmetric ternary circuits of depths (a) $N = 2$, (b) $N = 4$ and (c) $N = 6$ with the angles θ_k specified in Tab. IV. In each segment the scaling s^+ and wavelet b^+ , b^- sequences are plotted, which possess the number of vanishing moments (v.m.) denoted, together with the scaling and wavelet functions in the continuum limit (windowed to include only the non-vanishingly small part of the functions). The fourth panels on the right depict the Fourier transforms[9] of (upper) the scaling and wavelet sequences, and of (lower) the scaling and wavelet functions in the continuum limit.

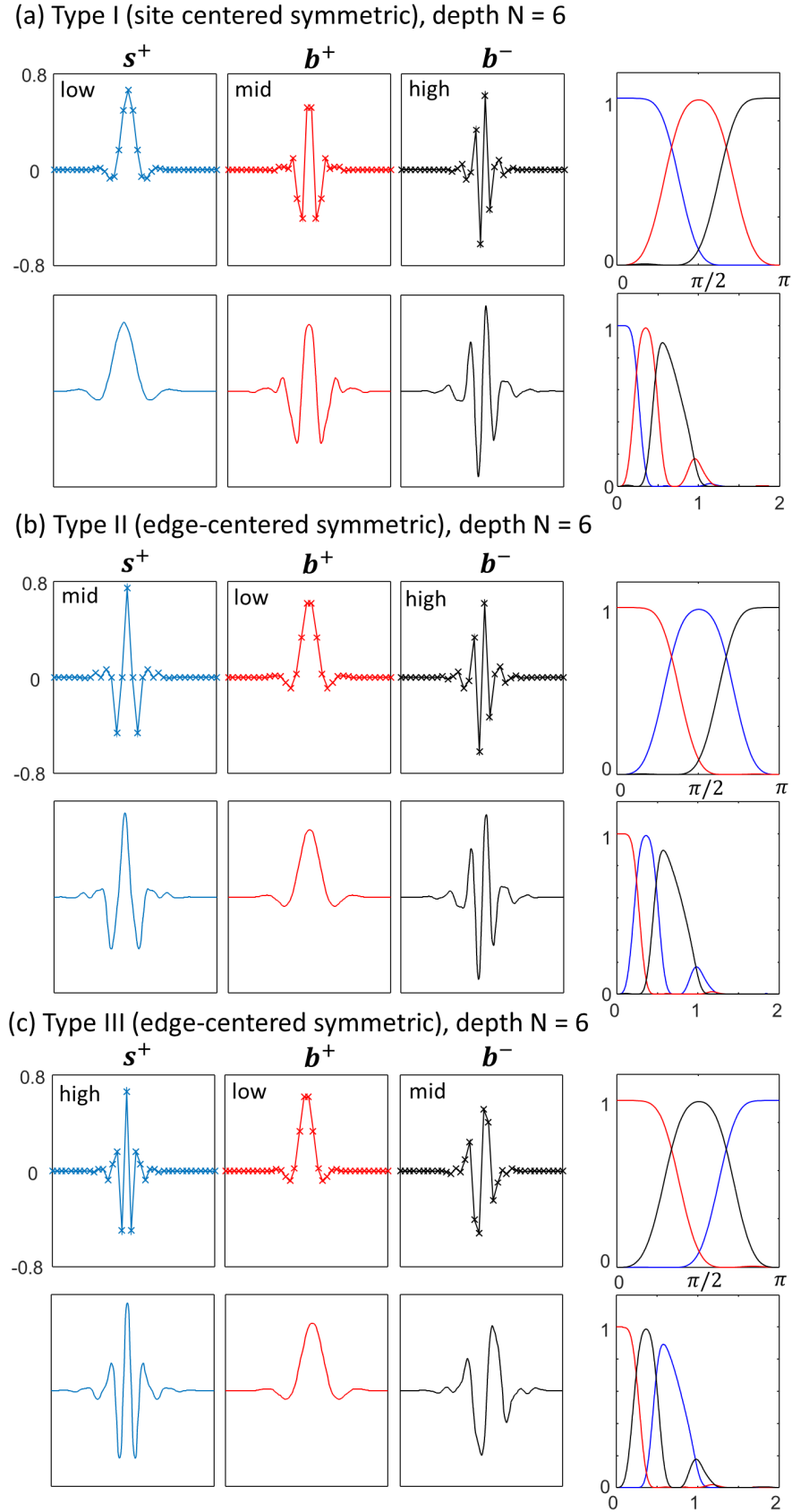


FIG. 8. Plots of the (a) Type I, (b) Type II and (c) Type III orthogonal wavelets, see Tab. V, from depth $N = 6$ ternary circuits with angles as given in Tab. VI. In each segment the three sequences s^+ , b^+ , b^- are plotted, together with the scaling and wavelet functions in the continuum limit (windowed to include only the non-vanishingly small part of the functions). The fourth panels on the right depict the fourier transforms of (upper) the scaling and wavelet sequences, and of (lower) the scaling and wavelet functions in the continuum limit. In all cases, each of level of the wavelet transform is well resolved into low (scaling), mid (wavelet) and high (wavelet) frequency components.

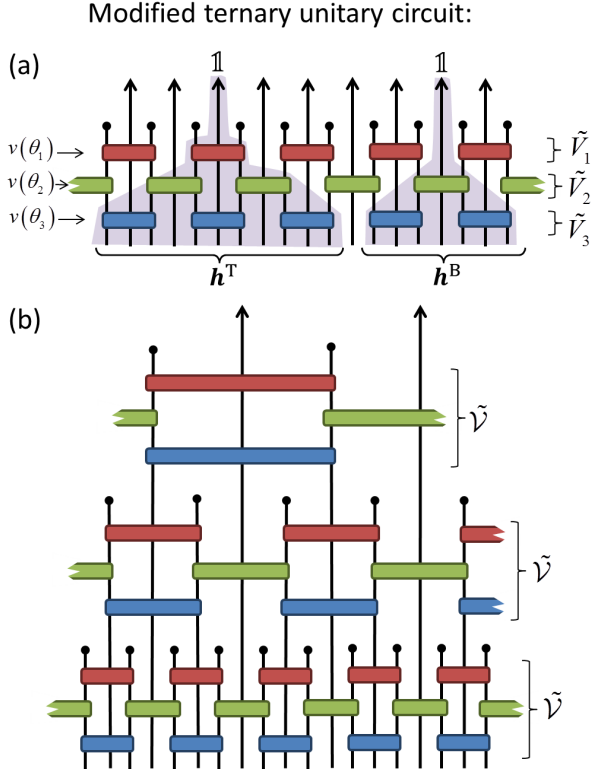


FIG. 9. (a) Depiction of a depth $N = 3$ modified ternary circuit, which is built from reflection symmetric 3×3 unitary matrices v and parameterized by angles $\{\theta_1, \theta_2, \theta_3\}$. Symmetric scaling sequences \mathbf{h}^T and \mathbf{h}^B are given from transforming unit vectors $\mathbb{1}$ located on the central index of $v(\theta_1)$ and $v(\theta_2)$ respectively. (b) Multi-scale circuit formed from composition of depth $N = 3$ modified ternary circuits.

see also Fig. 9(a), where each layer \tilde{V}_k is composed of a direct sum of 3×3 reflection symmetric unitary matrices $v(\theta_k)$, as defined in Eq. 40, that are spaced by single site identities \mathbb{I} ,

$$\tilde{V}_k = \dots \oplus v(\theta_k) \oplus \mathbb{I} \oplus v(\theta_k) \oplus \mathbb{I} \oplus v(\theta_k) \oplus \mathbb{I} \oplus \dots \quad (50)$$

Additionally we require that each layer \tilde{V}_k is offset by $r = 2$ sites from the proceeding layer. Notice that the depth N modified ternary circuit is parameterized by the set of angles $\{\theta_1, \theta_2, \dots, \theta_N\}$.

The modified ternary circuit \tilde{V} , which invariant under translations by four sites, may be interpreted as a four-channel filter bank. We label the four corresponding coefficient sequences \mathbf{h}^T , \mathbf{h}^B , \mathbf{g}^L and \mathbf{g}^R , each of which is given by transforming a unit vector, i.e. as $\langle \tilde{V} \times \mathbb{1}_r \rangle$. The sequences possesses the following properties,

- \mathbf{h}^T is a site-centered symmetric sequence of (odd) length $4N - 1$ elements (i.e. that is symmetric w.r.t. reflections about the central element), and is given from transforming the unit vector $\mathbb{1}$ located at the center of $v(\theta_1)$, see Fig. 9(a).
- \mathbf{h}^B is a site-centered symmetric sequence of (odd)

length $4N - 5$ elements (i.e. that is symmetric w.r.t. reflections about the central element), and is given from transforming the unit vector $\mathbb{1}$ located at the center of $v(\theta_2)$, see Fig. 9(a).

- \mathbf{g}^L and \mathbf{g}^R are length $4N - 1$ sequences given from transforming the unit vector $\mathbb{1}$ located at the left and right index of $v(\theta_2)$ respectively, and are related to each other by spatial reflection.

A multi-scale circuit can be formed by composition of modified ternary circuits, $\tilde{V} \circ \tilde{V} \circ \tilde{V} \circ \dots$, where both \mathbf{h}^T and \mathbf{h}^B are treated as scaling sequences, see also Fig. 9(b), which in turn represents the multiwavelet transform of dilation factor $m = 2$.

	$N = 4$	$N = 9$
θ_1	0.161653803	0.190056742
θ_2	0.389671265	0.438258716
θ_3	0.395157917	0.389371447
θ_4	0.167734951	-0.938456988
θ_5	-	0.319668509
θ_6	-	0.875926194
θ_7	-	-1.048336048
θ_8	-	0.314028313
θ_9	-	0.843502411

TABLE VII. Angles θ_k parameterizing depth $N = \{4, 9\}$ modified ternary circuits, see Fig. 9, that yield the wavelets depicted in Fig. 10.

2. Example 3: dilation $m = 2$ symmetric multi-wavelets

There are many possible criteria for optimization of the angles $\{\theta_1, \theta_2, \dots, \theta_N\}$ associated to the depth N modified ternary circuit \tilde{V} . One choice could be to optimize to maximize the number of vanishing moments that the wavelets possess. For instance, if angles θ_k were chosen such that the wavelet sequences \mathbf{g}^L and \mathbf{g}^R possessed vanishing moments, see Eq. 9, for $\alpha = [0, 1, \dots, P - 1]$ and the scaling sequences \mathbf{h}^T and \mathbf{h}^B had vanishing moments for $\alpha = [1, \dots, P - 1]$, then the family of multi-wavelets given from composition of \tilde{V} would possess P vanishing moments. Using this criteria we have found solutions for circuits depth $N = 3$ with $P = 2$ vanishing moments, and for depth $N = 6$ with $P = 4$ vanishing moments, although we do not present these results here.

Instead, in Tab. VII we present solutions for depth $N = 4$ with $P = 2$ vanishing moments, and for depth $N = 9$ with $P = 4$ vanishing moments. Here the extra degrees of freedom (resulting from use of larger depth N circuits than is necessary to achieve the desired number of vanishing moments) have been used to minimize the difference between the two distinct scaling sequences \mathbf{h}^T and \mathbf{h}^B of the multiwavelet transform, which also imposes that the wavelet sequences \mathbf{g}^L and \mathbf{g}^R are each in-

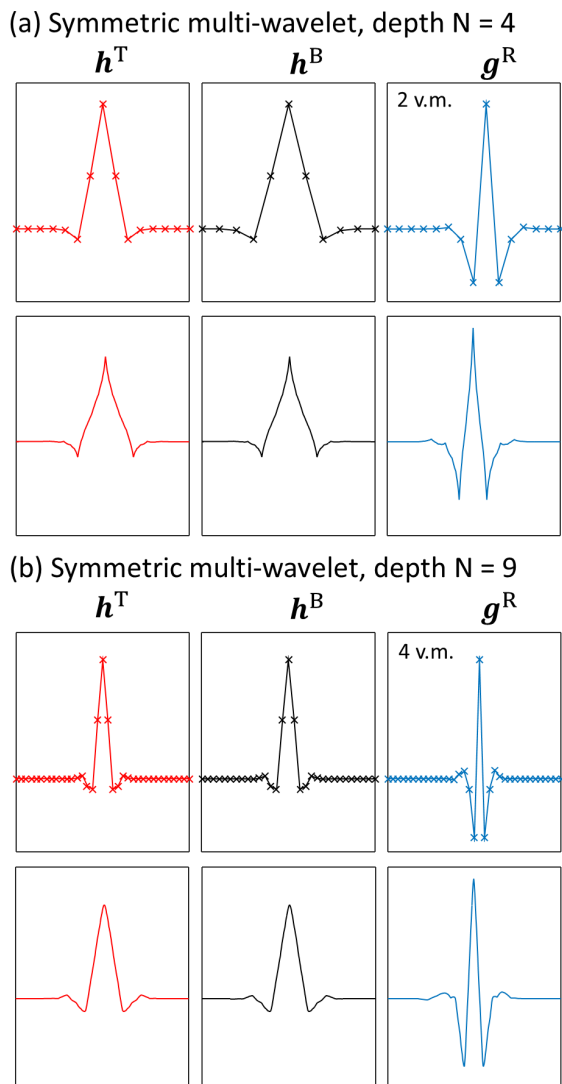


FIG. 10. Plots of orthogonal multi-wavelets from (a) depth $N = 4$ and (b) depth $N = 9$ modified ternary circuits with angles θ_k as given in Tab. VII. The top three panels of each group denote the (exactly symmetric) scaling sequences \mathbf{h}^T and \mathbf{h}^B , and the wavelet sequence \mathbf{g}^R (where \mathbf{g}^L , not shown, is the mirror of \mathbf{g}^R). The bottom three panels of each group depict the scaling functions and wavelets in the continuum limit (windowed to include only the non-vanishingly small part of the functions).

dividually close to being reflection symmetric. This was achieved using the Nelder-Mead algorithm to numerically optimize the angles $\{\theta_1, \theta_2, \dots, \theta_N\}$ as to minimize the magnitude of the desired scaling and wavelet sequence moments, as usual, but where a small term was also included in the figure of merits that penalized the difference between the two distinct scaling sequences. The term used was of the form $c\Omega$, where

$$\Omega = \|\mathbf{h}^T - \mathbf{h}^B\|, \quad (51)$$

and scalar c was a small fixed parameter. Note that the

sequence \mathbf{h}^B in Eq. 51 has been padded by two zero elements at the start and end of the sequence, such that the padded sequence is of the same length as \mathbf{h}^T .

The resulting wavelets are plotted in Fig. 10, which are seen to closely resemble the corresponding coiflets with $P = 2$ and $P = 4$ vanishing moments. In both examples only very small differences between the two scaling sequences are realized; for the depth $N = 4$ example we have $\|\mathbf{h}^T - \mathbf{h}^B\| = 0.0005$, while for the depth $N = 9$ example we have $\|\mathbf{h}^T - \mathbf{h}^B\| = 0.0048$. In comparison with coiflets, where the scaling functions are only approximately reflection symmetric, here we have achieved exact symmetry at the expense of now having two distinct (yet almost identical) scaling functions.

C. Dilation $m = 4$ symmetric wavelets

In this section we construct an example family of exactly reflection symmetric and antisymmetric wavelets of dilation factor $m = 4$ using a unitary circuit formalism. The purpose of this example is to demonstrate an alternate construction of symmetric wavelets that is not based upon the individually symmetric 3×3 unitary matrices $v(\theta)$ as considered in Sects. IV A and IV B. Instead, the circuit that represents the symmetric wavelet transform is built from 2×2 unitary matrices.

1. Quaternary circuits

Let \tilde{U} be a $4M \times 4M$ matrix for positive integer M ; we say that \tilde{U} is a depth N *quaternary unitary circuit* if it can be decomposed into N sublayers \tilde{U}_k , each of which is a direct sum of 2×2 unitary matrices u ,

$$\tilde{U}_k = \dots \oplus u(\theta_k) \oplus u(-\theta_k) \oplus u(\theta_k) \oplus u(-\theta_k) \oplus \dots, \quad (52)$$

where unitaries u are parameterized by a rotation angle θ_k , see Eq. 1, which alternates in sign with position, see also Fig. 11(a). Layers \tilde{U}_k of the quaternary unitary circuit \tilde{U} are inter-spaced with layers \tilde{U}_{sw} of swap gates,

$$\tilde{U}_{\text{sw}} = \dots \oplus u_{\text{sw}} \oplus u_{\text{sw}} \oplus u_{\text{sw}} \oplus u_{\text{sw}} \dots, \quad (53)$$

with u_{sw} the two site swap gate as defined in Eq. 38, and the quaternary circuit also includes a top sublayer \tilde{U}_{\pm} composed of 2×2 unitary gates $u(\pi/4)$,

$$\tilde{U}_{\pm} = \dots \oplus u(\pi/4) \oplus u(\pi/4) \oplus u(\pi/4) \dots, \quad (54)$$

Notice that the depth N quaternary unitary circuit is parameterized by the set of N angles $\{\theta_1, \theta_2, \dots, \theta_N\}$.

The quaternary unitary circuit, which is invariant w.r.t translations of four sites, may be interpreted as a four-channel filter bank. The four corresponding coefficient sequences $\{\mathbf{h}^+, \mathbf{h}^-, \mathbf{g}^+, \mathbf{g}^-\}$, each given from transforming the unit vector $\mathbb{1}_r$ on a non-equivalent site, have the following properties:

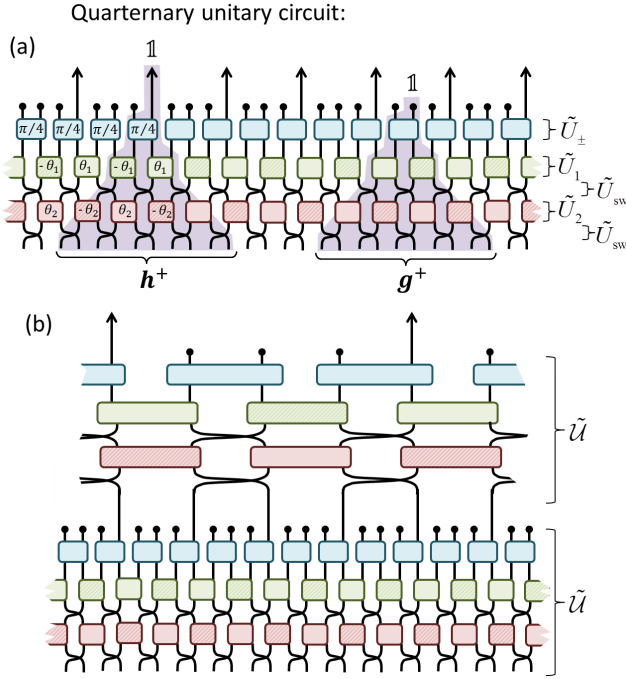


FIG. 11. (a) Depiction of a depth $N = 2$ quaternary circuit, which is built from 2×2 unitary matrices u and parameterized by angles $\{\theta_1, \theta_2\}$ as labelled. Symmetric sequences \mathbf{g}^+ and \mathbf{h}^+ are given from transforming unit vectors $\mathbb{1}$ located on a right-side index of an top level gate as indicated (while anti-symmetric sequences \mathbf{g}^- and \mathbf{h}^- are given from transforming unit vectors $\mathbb{1}$ located on a left-side index). (b) Multi-scale circuit formed from composition of depth $N = 3$ quaternary circuits.

- \mathbf{h}^+ is a edge-centered symmetric sequence of (even) length $4N + 2$ elements, given from transforming $\mathbb{1}_r$ with $r = 0, 4, 8, \dots$
- \mathbf{h}^- is a edge-centered antisymmetric sequence of (even) length $4N + 2$ elements, given from transforming $\mathbb{1}_r$ with $r = 1, 5, 9, \dots$
- \mathbf{g}^+ is a edge-centered symmetric sequence of (even) length $4N + 2$ elements, given from transforming $\mathbb{1}_r$ with $r = 2, 6, 10, \dots$
- \mathbf{g}^- is a edge-centered antisymmetric sequence of (even) length $4N + 2$ elements, given from transforming $\mathbb{1}_r$ with $r = 3, 7, 11, \dots$

The symmetry of the coefficient sequences can be understood by recalling that $\mathcal{R}(u(\theta)) = u(-\theta)$, where \mathcal{R} denotes spatial reflection, which implies that $(u(\theta) \oplus u(-\theta))$ constitutes a 4×4 unitary matrix that is reflection symmetric.

A multi-scale circuit, which represents a family of wavelet transform of dilation factor $m = 4$, is formed by composition $\tilde{U} \circ \tilde{U} \circ \tilde{U} \circ \dots$ of quaternary circuits, where \mathbf{h}^+ is treated as the scaling sequence, see also Fig. 11(b).

2. Example 4: dilation $m = 4$ symmetric wavelets

For a depth N quaternary circuit, we optimize the free angles $\{\theta_1, \theta_2, \dots, \theta_N\}$ numerically using the Nelder-Mead algorithm to give wavelet sequences $\{\mathbf{h}^-, \mathbf{g}^+, \mathbf{g}^-\}$ with as many vanishing moments as found to be possible. Two sets of example angles, one for depth $N = 4$ and the other for depth $N = 9$, are given in Tab. VIII. The depth $N = 4$ circuit yields wavelets with vanishing moments for orders $\alpha = [0, 1, 2]$, while the depth $N = 9$ circuit yields wavelets with vanishing moments for orders $\alpha = [0, 1, 2, 3, 4]$. These example wavelets, shown in Fig. 12, display a relatively high smoothness while also maintaining a small effective support, which suggests they may perform well in practical applications.

	$N = 4$	$N = 9$
θ_1	-1.229229752	2.807164665
θ_2	0.102977579	-0.473049662
θ_3	1.918752569	-1.482553131
θ_4	-0.198852925	-1.922365069
θ_5	-	-3.091128284
θ_6	-	2.257247480
θ_7	-	2.554082219
θ_8	-	-0.492838196
θ_9	-	-0.633172753

TABLE VIII. Angles parameterizing depth $N = 4, 9$ quaternary circuits, as depicted in Fig. 11, which produce the wavelets depicted in Fig. 12.

D. Boundary wavelets

In this section we explore the use of unitary circuits in the construction of boundary wavelets[36–39], using a similar approach to the boundary MERA developed in the context of studying quantum spin chains with open boundaries[26, 27].

1. Example 5: boundary wavelets for D4 Daubechies wavelets

Here we provide an example the use of a unitary circuit in the construction of boundary wavelets for the specific case of the D4 Daubechies wavelets, although the general strategy we employ for constructing the boundary wavelets can easily be extended not only to higher order Daubechies wavelets, but also to other wavelet families. The boundary wavelets we construct are orthogonal and, as with the D4 Daubechies wavelets, possess two vanishing moments.

The boundary wavelets are parameterized using a *boundary unitary circuit*, see Fig. 13, which is con-

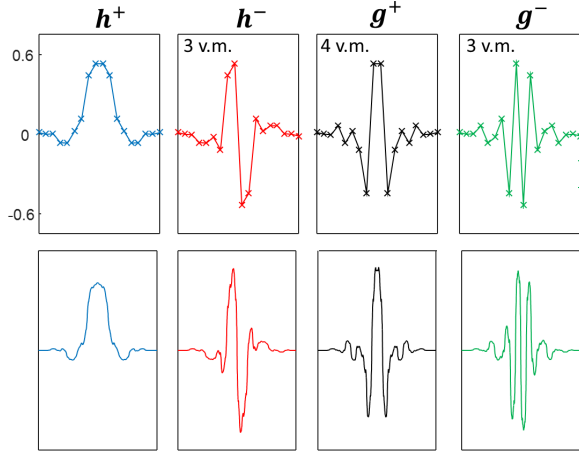
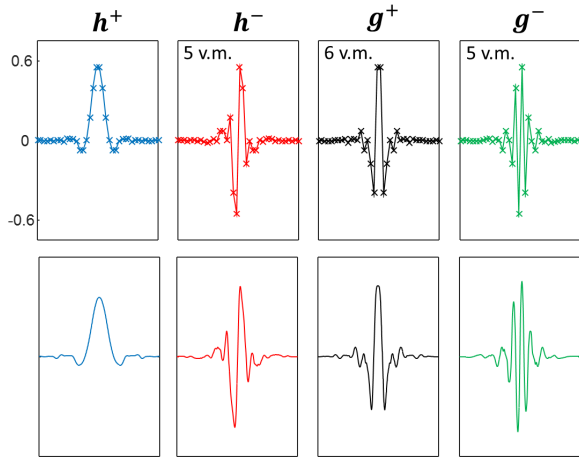
(a) Dilation factor 4, symmetric, depth $N = 4$ (b) Dilation factor 4, symmetric, depth $N = 9$ 

FIG. 12. Plots of dilation $m = 4$ orthogonal wavelets from (a) depth $N = 4$ and (b) depth $N = 9$ quaternary circuits with angles θ_k as given in Tab. VIII. The top three panels of each group denote the (exactly symmetric) scaling sequence h^+ and wavelet sequences h^- , g^+ , h^- , which possess the number of vanishing moments (v.m.) as indicated. The bottom three panels of each group depict the scaling functions and wavelets in the continuum limit (windowed to include only the non-vanishingly small part of the functions).

structed as follows. Let \mathcal{L} be a semi-infinite lattice of sites $r = [1, 2, 3, \dots]$, i.e. with an open boundary on the left. We apply as much of the multi-scale circuit corresponding to the D4 wavelets, i.e. composed of depth $N = 2$ binary unitary circuits with angles $\theta_1 = 5\pi/12$ and $\theta_2 = \pi/6$ (see Sect. IIIB), that can be supported on \mathcal{L} . Then a double layer of scale-dependent 2×2 unitary gates, parameterized by angles $\{\phi_1, \phi_2, \phi_3, \dots\}$ and $\{\sigma_1, \sigma_2, \sigma_3, \dots\}$, where subscripts here denote scale z , is introduced on the boundary of the multi-scale circuit.

Starting from the lowest scale the angles ϕ_1 and σ_1 are fixed such that the corresponding boundary wavelet g^B at that scale, as depicted in Fig. 13(a), has two vanish-

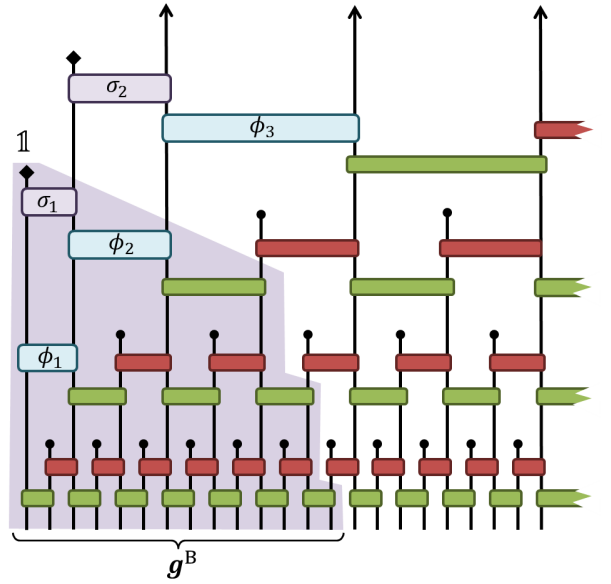


FIG. 13. Depiction of a multi-scale circuit (formed from composition of depth $N = 2$ binary unitary circuits) with an open boundary on the left, where a double layer of (scale dependent) unitary gates $u(\phi_z)$ and $u(\sigma_z)$ is introduced. Boundary wavelets g^B are given by transforming the unit vector $\mathbb{1}$ located on a boundary index as indicated. The angles ϕ_z and σ_z are chosen to ensure the boundary wavelets each have two vanishing moments.

	ϕ_z	σ_z
$z = 1$	0.615479708	0.261157410
$z = 2$	0.713724378	0.316335000
$z = 3$	0.752040089	0.339836909
$z = 4$	0.769266332	0.350823961
$z = 5$	0.777461322	0.356148400
$z = 6$	0.781461114	0.358770670
$z = 7$	0.783437374	0.360072087
$z = 8$	0.784419689	0.360720398
$z = 9$	0.784909404	0.361043958
$z = 10$	0.785153903	0.361205590
$z = 11$	0.785276063	0.361286369
$z = 12$	0.785337120	0.361326749

TABLE IX. Angles ϕ_z and σ_z parameterizing the boundary unitary gates at scale z , see Fig. 13, of the boundary D4 Daubechies wavelets.

ing moments. Here the angles ϕ_1 and σ_1 can be found deterministically using a algorithm similar to the circuit construction algorithm discussed in Sect. IIIC2. We then apply the algorithm iteratively, scale-by-scale, to fix remaining angles $\{\phi_2, \phi_3, \dots\}$ and $\{\sigma_2, \sigma_3, \dots\}$ such that all boundary wavelets have two vanishing moments. The resulting angles are given in Tab. IX, and are seen to converge to the values $\phi_z = \pi/4$ and $\sigma_z = 0.361367123906708$ in the large scale limit, $z \rightarrow \infty$.

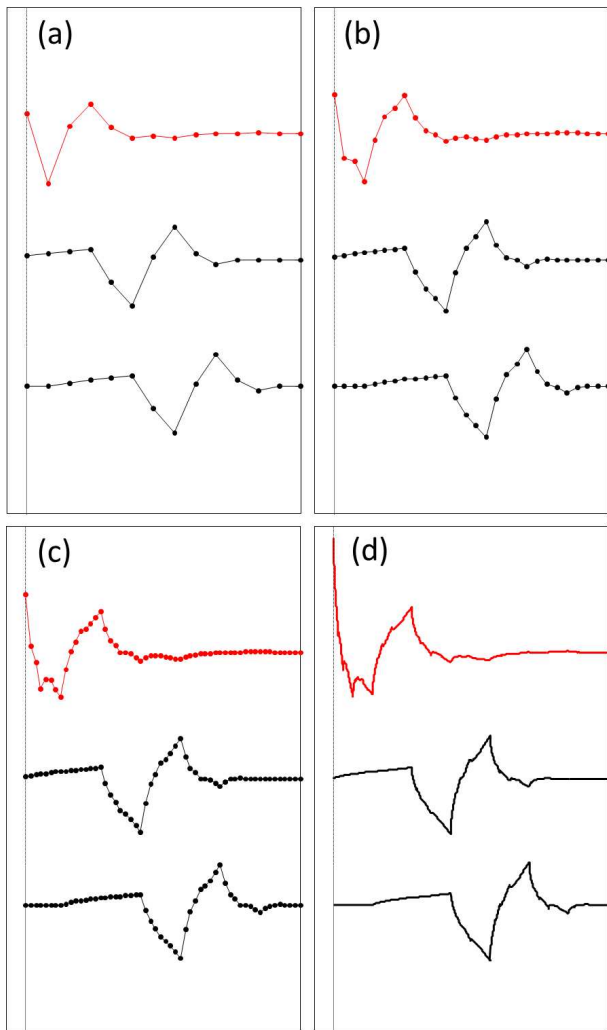


FIG. 14. Plots of the orthogonal boundary wavelet (red) and two of the bulk D4 Daubechies wavelets at the same scale (black) from the boundary unitary circuit depicted in Fig. 13, with the angles as specified in Tab. IX for (a) scale $z = 1$, (b) scale $z = 2$, (c) scale $z = 3$ and (d) the continuum limit. All wavelets are orthogonal and have two vanishing moments.

The resulting boundary wavelets are plotted in Fig. 14 over several different scales z . Notice that the double layer of unitary gates was used in the boundary circuit of Fig. 14 in order to provide two degrees of freedom ϕ_z and σ_z for each boundary wavelet (which could then be chosen in order to endow each boundary wavelet with two vanishing moments). More generally additional layers of boundary unitary gates could be included in order to generate wavelets with higher vanishing moments.

E. Biorthogonal wavelets

Biorthogonal wavelets, such as the CDF wavelets introduced in Ref. 5, follow from removing the orthogonality constraint on wavelets while still requiring per-

fect reconstruction. For a given number of vanishing moments, biorthogonal wavelets can possess smaller support than orthogonal wavelets, and can be exactly symmetric even for dilation factor $m = 2$. These properties make biorthogonal wavelets useful in practical applications such as image compression, where they are employed in the JPEG2000 format [12].

In this section we briefly discuss the use of a circuit formalism in the construction of biorthogonal wavelets. First we introduce the notion of invertible circuits which are built from many copies of local invertible matrices, and follow from relaxing the unitary constraint on the circuit formalism. As with the case of the unitary circuits explored in this manuscript, many different forms of invertible circuit could be considered; here the example we provide leads to a novel family of (edge-centered) antisymmetric biorthogonal wavelets.

1. Binary invertible circuits

We consider a circuit with the same structure as the binary unitary circuits considered in Sect. II, but where the unitary constraint on the 2×2 matrices has been removed, and instead the matrices are constrained to be reflection symmetric. Let $a(\mu)$ be a 2×2 reflection symmetric matrix parameterized by real parameter μ ,

$$a(\mu) = \begin{bmatrix} 1 & \mu \\ \mu & 1 \end{bmatrix}, \quad |\mu| \neq 1, \quad (55)$$

and let \mathcal{A} be an invertible matrix of dimension $2M \times 2M$ for integer M . We say that \mathcal{A} is a *binary invertible circuit* of depth N if it can be decomposed into sublayers,

$$\mathcal{A} = A_N A_{N-1} \dots A_2 A_1 \tilde{U}_{\pm}, \quad (56)$$

see also Fig. 15(a), where \tilde{U}_{\pm} is a direct sum of unitary gates $u(\pi/4)$ as defined in Eq. 54. Here A_k is a $2M \times 2M$ matrix given as the direct sum of M matrices $a(\mu)$,

$$A_k = \dots \oplus a(\mu_k) \oplus a(\mu_k) \oplus a(\mu_k) \oplus \dots, \quad (57)$$

and each sublayer A_k is offset by one site from the preceding sublayer. Notice that the depth N circuit \mathcal{A} is parameterized by the N real numbers $\{\mu_1, \mu_2, \dots, \mu_N\}$ restricted such that $|\mu_k| \neq 1$.

We wish to interpret the binary invertible circuit \mathcal{A} as the *decomposition* part of a two-channel filter bank. Let \mathbf{q} be a vector of length $2M$, which we transform to new vector \mathbf{p} using the binary invertible circuit \mathcal{A} ,

$$\mathbf{q}^\dagger \mathcal{A} = \mathbf{p}^\dagger. \quad (58)$$

The original vector \mathbf{q} can be reconstructed from \mathbf{p} as,

$$(\mathcal{A}^\dagger)^{-1} \mathbf{p} = \mathbf{q}, \quad (59)$$

where $(\mathcal{A}^\dagger)^{-1}$, which we refer to as the dual of \mathcal{A} , is the *corresponding* reconstruction part of a two-channel filter bank.

Let us now examine the form of the dual circuit. The inverse-transpose can be taken of each sublayer individually,

$$(\mathcal{A}^\dagger)^{-1} = (A_N^\dagger)^{-1} \dots (A_2^\dagger)^{-1} (A_1^\dagger)^{-1} \tilde{U}_\pm, \quad (60)$$

where again each sublayer $(A_k^\dagger)^{-1}$ is offset by one site from the preceding sublayer, see also Fig. 15(b). Notice that the transpose of \tilde{U}_\pm is its own inverse. Similarly, since it can be shown that (for $|\mu| \neq 1$),

$$a(\mu)^{-1} \propto \begin{bmatrix} 1 & -\mu \\ -\mu & 1 \end{bmatrix} \quad (61)$$

$$= a(-\mu), \quad (62)$$

it follows that $(A_k^\dagger)^{-1}$ is given as the direct sum of M matrices $a(-\mu)$,

$$(A_k^\dagger)^{-1} \propto a(-\mu_k) \oplus a(-\mu_k) \oplus a(-\mu_k) \oplus \dots, \quad (63)$$

We label the (decomposition) scaling and wavelet sequences as \mathbf{h}^d and \mathbf{g}^d respectively, which are given from $\langle \mathcal{A} \times \mathbb{1}_r \rangle$, and the (reconstruction) scaling and wavelet sequences as \mathbf{h}^r and \mathbf{g}^r respectively, which are given from $\langle (\mathcal{A}^\dagger)^{-1} \times \mathbb{1}_r \rangle$, see also Fig. 15(a-b). These coefficient sequences have the following properties:

- \mathbf{h}^d and \mathbf{h}^r are a edge-centered symmetric sequences of (even) length $2N + 2$ elements.
- \mathbf{g}^d and \mathbf{g}^r are a edge-centered antisymmetric sequences of (even) length $2N + 2$ elements.

Once again the binary invertible circuit can be composed to form a multi-scale circuit,

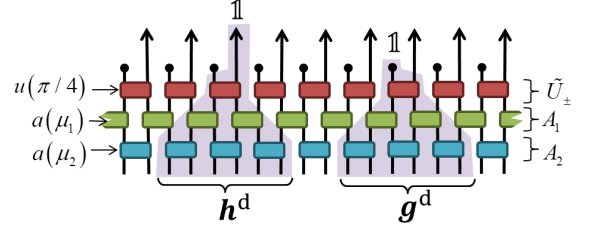
$$\mathcal{A} \circ \mathcal{A} \circ \mathcal{A} \circ \mathcal{A} \circ \dots, \quad (64)$$

see also Fig. 15(c), which encodes a family of antisymmetric biorthogonal wavelets of dilation factor $m = 2$.

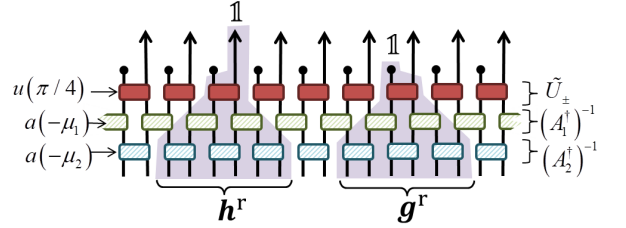
2. Example 6: edge-centered symmetric biorthogonal wavelets

Here we provide an example of biorthogonal wavelets constructed using a binary invertible circuit. For a depth $N = 4$ binary invertible circuit we use algebraic methods to fix the parameters $\{\mu_1, \mu_2, \mu_3, \mu_4\}$, see Tab. X, such that both the decomposition \mathbf{g}^d and reconstruction \mathbf{g}^r wavelets have vanishing moments for $\alpha = [0, 1, 2, 3, 4]$. The resulting antisymmetric wavelets are depicted in Fig. 16.

(a) Binary invertible circuit (decomposition):



(b) Binary invertible circuit (reconstruction):



(c)

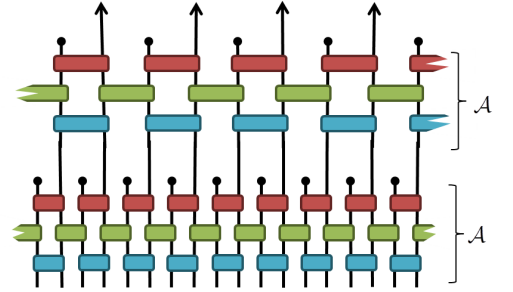


FIG. 15. (a) Decomposition binary invertible circuit \mathcal{A} of depth $N = 2$, see Eq. 56. Layers A_k are composed of a direct sum of 2×2 invertible symmetric matrices a of Eq. 55, while layers \tilde{U}_\pm are composed of two site unitary gates u . Transforming a unit vector $\mathbb{1}$ gives either the symmetric scaling sequence \mathbf{h}^d or antisymmetric wavelet sequence \mathbf{g}^d . (b) Reconstruction binary invertible circuit $(\mathcal{A}^\dagger)^{-1}$ for the circuit in (a). Reconstruction scaling \mathbf{h}^r and wavelet \mathbf{g}^r sequences are shown. (c) Multi-scale circuit formed from composition of the binary invertible circuit \mathcal{A} of (a).

V. CONCLUSIONS

The main objective of this manuscript was to recast wavelets in the circuit formalism familiar to multi-scale methods used for simulating quantum many-body systems, thereby further elaborating on the connection established in Ref. 2. In the context of quantum many-body physics, this connection is useful in allowing the derivation of wavelet-based quantum circuits for describing the efficient preparation of ground states of certain many-body systems on a quantum computer. The connection between wavelets and unitary circuits has also been exploited in Ref. 40 to produce the first analytic error bounds for the accuracy of MERA representations of ground states in $D = 1, 2$ dimensional quantum sys-

	$N = 4$
μ_1	-0.25684952118
μ_2	0.85058116979
μ_3	0.05040158211
μ_4	-0.83314630482

TABLE X. Parameters defining the depth $N = 4$ binary invertible circuit, as depicted in Fig. 15, which produce the wavelets depicted in Fig. 16.

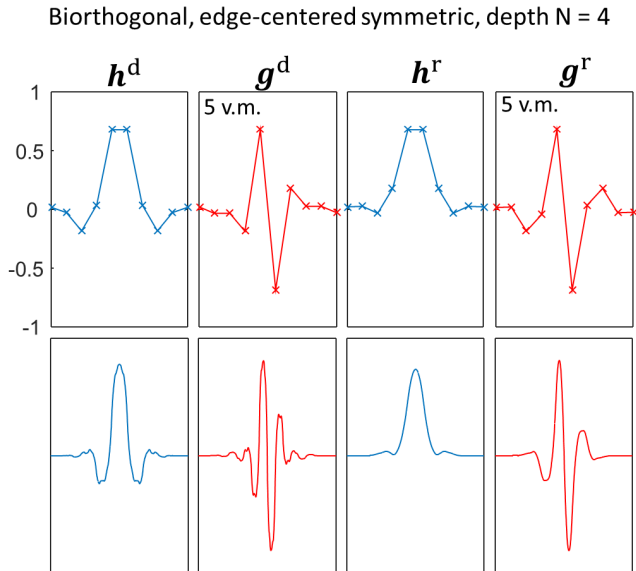


FIG. 16. (Top) Plots of the decomposition scaling h^d and wavelet g^d sequences, and reconstruction scaling h^r and wavelet g^r sequences, given from a depth $N = 4$ binary invertible circuit with parameters μ_k as specified in Tab. X. Both wavelet sequences possess 5 vanishing moments (v.m.). (Bottom) The corresponding scaling functions and wavelets in the continuum limit.

tems. In addition, some of the new families of symmetric wavelet developed in this manuscript have been used in the construction of improved basis sets for electronic structure calculations [41].

The representation of common orthogonal wavelet families, such as Daubechies wavelets, symlets and coiflets, as unitary circuits composed of 2×2 rotation matrices, which are parameterized by rotation angles θ_k , appears to be a very natural one. The circuit representation makes explicit key properties of the wavelets (such as orthogonality), facilitates in the understanding of aspects of

their construction (such as the cascade algorithm), and is amenable to their efficient numeric implementation. Furthermore, as evidenced in Tabs. I, II and III and Fig. 4, parameterization in terms of rotation angles affirms a clear-cut relation between different orders of wavelets within the same family.

As demonstrated throughout the manuscript, the circuit formalism can be useful in the design of novel wavelet transforms. The families of wavelets given in Sect. IV were constructed via a two-step process that involved (i) the design of the circuit that builds desired properties into the parameterization (e.g. orthogonality, symmetry, dilation factor) and (ii) numerical optimization of the parameters according to some specified criteria (e.g. to achieve the maximal number of vanishing moments). Interestingly, these are the same two steps involved in the implementation of MERA for the study of quantum many-body systems, where the criteria for the numerical optimization in (ii) then involves minimizing the energy of the MERA with respect to a system Hamiltonian. In most of the examples presented in this manuscript the Nelder-Mead algorithm, a standard numeric algorithm for minimizing a multi-dimensional objective function, was used in the optimization of the circuit parameters, although more sophisticated numerical or analytic methods could, in general, also be employed.

The examples provided were intended to demonstrate the utility of the circuit formalism in wavelet design, but certainly do not constitute an exhaustive list of the wavelets that can be constructed using this approach. For each of the circuit examples provided, one could straight-forwardly consider higher order wavelets based on larger depth circuits, as well as alternative optimization criteria for the free parameters θ_k of the circuits. Many other circuit designs are also possible, including circuits in higher dimensions, analogous to higher dimensional implementations of MERA[19, 23], which could represent novel families of non-separable orthogonal $2D$ (or $3D$) wavelets. Despite only intending to serve as examples, many of the wavelets given appear to perform well in practical applications. Though not presented in this manuscript, preliminary investigations suggest that the wavelets described in examples 2, 3 and 6 perform similarly to, or in some cases exceed the performance of, the CDF-9/7 wavelets in application to image compression. The use of circuits in optimal wavelet design for specific applications remains an interesting direction for future research.

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